

PATENT ABSTRACTS OF JAPAN

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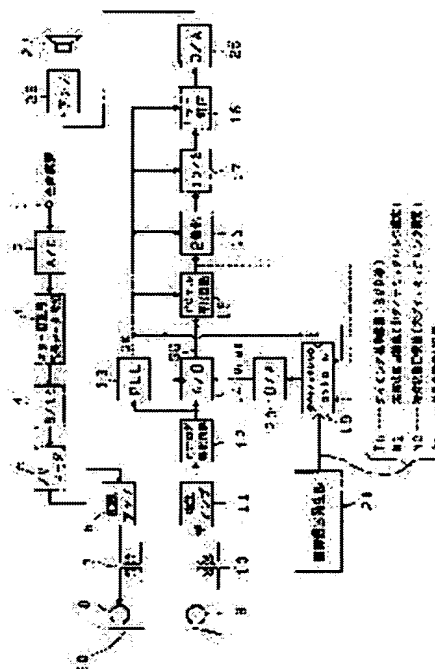
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(54) DATA REPRODUCING EQUIPMENT

(57)Abstract:

PROBLEM TO BE SOLVED: To lessen an error by making a control so that a dynamic range be made small when an operation of data reproducing equipment is in a steady state and that the dynamic range be made large when the operation is in a specific state.

SOLUTION: In this data reproducing equipment, a dynamic range of an A/D converter 14 is made small in a steady state wherein an input signal is stable in a certain degree and thereby a quantization error is lessened, so that an error rate be improved. At the time when there is the possibility that an input signal to the A/D converter 14 changes suddenly, e.g. at the time of search, a change in a mode or others, on the other hand, the dynamic range of the A/D converter 14 is made large, even though the quantization error is allowed in a certain degree, and thereby a sufficient saturation margin is secured so that an overflow may not occur. According to this constitution, an extreme increase of an error is prevented.



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CLAIMS

[Claim(s)]

[Claim 1]In a data reproduction apparatus which decodes by changing into digital data an RF signal read from a recording medium by an A/D conversion means, and reproduces data, Have a dynamic range control means which can carry out variable control of the dynamic range in said A/D conversion means, and this dynamic range control means, A data reproduction apparatus controlling to enlarge a dynamic range when it is small in a dynamic range when operation of the data reproduction apparatus concerned is a stationary state, and operation of the data reproduction apparatus concerned is in a special state.

[Claim 2]The data reproduction apparatus according to claim 1 using a time of being in said special state with a prescribed period when a period and/or operational mode to which the data reproduction apparatus concerned is performing a search operation change.

[Claim 3]In a data reproduction apparatus which decodes by changing into digital data an RF signal read from a recording medium by an A/D conversion means, and reproduces data, It has a dynamic range control means which can carry out variable control of the dynamic range in said A/D conversion means accommodative according to an output of said A/D conversion means, This dynamic range control means is set up so that the response of dynamic range variable control operation according to an output of said A/D conversion means may become late, when operation of the data reproduction apparatus concerned is a stationary state, A data reproduction apparatus setting up so that the response of dynamic range variable control operation according to an output of said A/D conversion means may become early, when operation of the data reproduction apparatus concerned is in a special state.

[Claim 4]The data reproduction apparatus according to claim 3 using a time of being in said special state with a prescribed period when a period and/or operational mode to which the data reproduction apparatus concerned is performing a search operation change.

[Claim 5]In a data reproduction apparatus which decodes by changing into digital data an RF signal read from a recording medium by an A/D conversion means, and reproduces data, It has a dynamic range control means which can carry out variable control of the dynamic range in said A/D conversion means accommodative according to an output of said A/D conversion means, A data reproduction apparatus, wherein this dynamic range control means is set up so that the response of dynamic range variable control operation according to an output of said A/D conversion means may become early when it performs control to which a dynamic range of said A/D conversion means is expanded.

[Claim 6]In a data reproduction apparatus which changes into digital data an RF signal read from a recording medium by an A/D conversion means, decodes after performing equalization processing by an equalization means, and reproduces data, A data reproduction apparatus having supervised both an output of said A/D conversion means, and an output of said equalization means, and having a dynamic range control means which can carry out variable control of the dynamic range in said A/D conversion means accommodative.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention changes into digital data the signal read from the recording medium, performs equalization processing and decoding, and relates to the data reproduction apparatus which reproduces data.

[0002]

[Description of the Prior Art]Various kinds of recording media, such as magnetic tape, a magnetic disk, an optical disc, and a magneto-optical disc, and the recording and reproducing device corresponding to it have spread. In the playback equipment in a high-density digital recording system in recent years, the A/D conversion of a deed and the RF signal by which equalization was carried out is carried out for the equalization processing by the analog equalizer or a digital filter to the signal (RF signal) read from the recording medium by the playback head. And equalization processing, binarization processing, decoding, error correction processing, etc. are performed to digital data, and data is reproduced in many cases. This an equalization method as RF signal treatment technique of a high-density digital recording system A partial response method, It is because the example which adopts the combination (PRML method) of a maximum likelihood decoding method (Viterbi decoding: Viterbi detection : Maximum Likelyhood Detection Method) for a detection system is increasing.

[0003]For example, performed binary-ization, when the DAT (digital audio tape) recording and reproducing device was mentioned as the example, as RF processing, by the analog limiting circuit, old adopted integration equalization, are easy composition of decoding and an error correction, and were ending, but. Since the Viterbi detecting operation is the structure which binary-izes the detecting point voltage system sequence (sampling-data series) of the RF signal by which equalization was carried out by carrying out digital signal processing when a PRML method is adopted, the A/D converter for sampling an RF signal is needed.

[0004]However, it has a dynamic range peculiar as a signal input range in which an analog to digital is possible, when an input signal level is not an appropriate range compared with a dynamic range, good sample data is not obtained, but the situation where detection errors occur frequently produces an A/D converter.

[0005]That is, when the RF signal of remarkable small amplitude is inputted compared with a dynamic range, the quantization error under output (sample data) of an A/D converter increases, and since the signal to noise ratio gets worse, a detection error increases. When the RF signal of large amplitude which exceeds a dynamic range is inputted, sample data will turn into saturated data, namely, the linearity in A/D conversion operation will be spoiled. The signal to noise ratio of such sample data has deteriorated in the degree very much, and a detection error increases substantially.

[0006]Drawing 12 - drawing 25 explain these situations. An RF signal is explained that it is the waveform by which equalization was carried out by the class 1 partial-response method (PR (1, 1) method). Drawing 12 is an eye pattern of a class 1 partial-response-equalization waveform. This equalization waveform can take three kinds of values, "1", "0", and "-1", with the sample point (detecting point) shown by O in a figure. However, since an actual waveform contains a

noise, as shown in this figure, it does not converge on one point with a sample point, and it varies.

[0007]A sampling of such a waveform will acquire the sample data distribution distributed focusing on three voltage like drawing 13. In a 30000-point table, this drawing 13 is the shown graph about the sample data value (pressure value) which sampled the RF signal with the A/D converter. This is in a state as shown the dynamic range of an A/D converter in the schematic diagram 14, when the accuracy of an A/D converter is 8 bits (-128 – $+127$) and it sets up. That is, it is a case where it is assumed that the saturation margin of a certain grade is taken as a dynamic range of an A/D converter to the amplitude (slash part) of an RF signal waveform like drawing 14, and the dynamic range of an A/D converter is generally set as a proper state to RF signal amplitude. In such a case, sampling-data distribution of about ~ 100 points was acquired like drawing 13.

[0008]Next, the case where RF signal voltage (amplitude) becomes half mostly like drawing 15 compared with drawing 14 is considered. The sample data distribution at this time becomes like drawing 16. The same scale as said drawing 13 shows the graph of drawing 16, and drawing 17 expanded this. Sample data distribution turns into distribution of the range of about ~ 50 points, especially sample data distribution is sparse so that drawing 17 may be compared and understood to drawing 13, so that drawing 16 may show. This means that the quantization error is increasing because RF signal amplitude becomes small to the dynamic range of an A/D converter.

[0009]Distribution when RF signal voltage (amplitude) becomes about $1/4$, and the abbreviation $1/8$ compared with the state of drawing 14 is shown in drawing 18 and drawing 20, respectively. The same scale as said drawing 13 shows drawing 18 and drawing 20, and that to which having expanded drawing 18 expanded drawing 19 and drawing 20 is drawing 21. From these figures, it is understood that a quantization error increases, so that it is observed that sample data distribution is still more sparse, that is, RF signal amplitude becomes small to the dynamic range of an A/D converter.

[0010]Next, the case where it becomes the thing that RF signal amplitude exceeds the dynamic range of an A/D converter is considered. Drawing 22 shows distribution of the sample data at the time of setting up the dynamic range of an A/D converter, as shown in drawing 23. That is, compared with the case where the dynamic range is standard like drawing 14, RF signal amplitude is an example used as about 1.5 time. In the distribution state of drawing 22, the maximum of the value of sample data is restricted to $+127$, the minimum is restricted to -128 , and being saturated is observed. RF signal voltage is only about 1.5. Although becoming change which double size hears was only carried out, the linearity of A/D conversion operation is spoiled by this. And normal operation of the Viterbi decoding will not be carried out to such a sample data series, but errors will occur frequently.

[0011]Furthermore, drawing 24 shows distribution of the sample data at the time of setting up the dynamic range of an A/D converter, as shown in drawing 25. This is the example from which RF signal amplitude became twice [about] compared with the case where the dynamic range is standard like drawing 14. The maximum of the value of sample data having been restricted to $+127$, and the minimum having been restricted to -128 , and being saturated also with the distribution state of this drawing 24 is observed. And when RF signal voltage becomes large twice [about], the linearity of A/D conversion operation will be spoiled greatly, and normal operation of the Viterbi decoding will not be carried out to such a sample data series, but errors will occur frequently more.

[0012]When an input signal level is not an appropriate range compared with a dynamic range as mentioned above, good sample data will not be obtained from an A/D converter, but detection errors will occur frequently. These people performed the proposal indicated to Japanese Patent Application No. No. 183945 [six to] as advanced technology to such a situation. The art which uses an input signal as a suitable level to the dynamic range of an A/D converter by establishing the AGC circuit (automatic gain control circuit) which controls the input level of an A/D converter according to the output of an A/D converter in this Japanese Patent Application No. No. 183945 [six to] is indicated.

[0013]

[Problem(s) to be Solved by the Invention]The following problems are left behind although the input signal level to the dynamic range of an A/D converter can usually be made into an appropriate range by providing the AGC circuit to the input signal of an A/D converter.

[0014]In playback equipment, when operational modes, such as reproduction motion and a search operation, change, reproduction motion rushes into an existing recording part from the non-recording part on a recording medium, and reproduction motion rushes into a non-recording part from the existing recording part on a recording medium, an RF signal level may be changed sharply.

[0015]Although it is required also for the sudden amplitude increase which is produced as the dynamic range of the A/D converter mentioned above, and a relation of an input signal level in such a case to make management possible, it is required to set up a dynamic range more greatly beforehand for the purpose. That is, it is giving a saturation margin. However, in such a case, it is also that a quantization error increases. That is, two requirements of [usually follow only by the input level control at the time, and] reduction in a quantization error and the correspondence to sudden large amplitude by an AGC circuit cannot be satisfied.

[0016]If the response performance of an AGC circuit is considered about the time of sudden change of input signal amplitude, the following problems will arise. Since AGC control is carried out so that a small level signal may be in a proper state to the dynamic range of an A/D converter till then when RF signal amplitude changes from a small level to a large level suddenly first, at the time of a sudden large amplitude input, a dynamic range will become [too little] relatively. Therefore, since sample data is saturated by the period until an AGC circuit lowers a gain to a proper state corresponding to a large amplitude input, the signal to noise ratio deteriorates greatly and an error increases it to a degree very much. Therefore, an AGC circuit is asked for quick response performance so that it can answer immediately at large amplitude in such a case.

[0017]Since it is in the state where the dynamic range is adapted for the large amplitude RF signal till then when RF signal amplitude changes from a large level to a small level suddenly, a dynamic range will become excessive relatively to a small level input. For this reason, a quantization error increases and degradation of the signal to noise ratio and increase of an error arise also in this case. Therefore, an AGC circuit is asked for quick response performance also in this case.

[0018]However, if speed of response is sped up, convergency will worsen and an AGC loop will become unstable. For this reason, high speed response-ization was not able to be performed, so that it could respond to the sudden amplitude change enough. And in the apparatus to which operational modes, such as reproduction/search, change from the difficult situation of high-speed-response-izing frequently like computer data storage apparatus, it became disadvantageous especially. That is, it is because an overhead until an AGC circuit is stabilized becomes long and the reaction velocity of apparatus becomes slow by this.

[0019]Considering the device furthermore provided with the digital equalizing circuit, even if sample data is not saturated with the output stage story of an A/D converter, there is a possibility that overflow may arise to data by the operation of a digital equalizing circuit. Since change of an equalization characteristic cannot be predicted in the case of the apparatus which adjusts especially an equalization characteristic automatically (adaptive equalization), supervising also about the output signal of an equalizing circuit is called for.

[0020]

[Means for Solving the Problem]While this invention presupposes that it is controllable so that a dynamic range and an input signal level of an A/D conversion means may be in an always suitable state in view of the above problems, conflicting requirements of making small enlarging a dynamic range of an A/D conversion means and acquiring a saturation margin, and a quantization error -- a case -- a division -- being able to be satisfied -- making -- things. opposite requirements of the stability of a control loop, and improvement in the speed of speed of response -- a case -- a division -- being able to be satisfied -- making -- things. When required, in performing giving priority to a measure against saturation over a measure against a

quantization error, and digital equalization, it aims at realizing prevention from saturation in the digital equalization processing.

[0021] For this reason, have a dynamic range control means which can carry out variable control of the dynamic range in an A/D conversion means first, and this dynamic range control means, When operation of the data reproduction apparatus concerned is a stationary state, it is small in a dynamic range, and it controls to enlarge a dynamic range, when operation of the data reproduction apparatus concerned is in a special state. That is, while carrying out variable control of the dynamic range so that a dynamic range and an input signal level of an A/D conversion means may be in an always suitable state, Although a sudden amplitude change makes a dynamic range of an A/D conversion means small and makes a quantization error small in a stationary state considered to hardly generate, In the special state where there is a possibility that a sudden amplitude change may occur, a dynamic range is enlarged, a saturation margin is enlarged and overflow is prevented.

[0022] It has a dynamic range control means which can carry out variable control of the dynamic range in an A/D conversion means accommodative according to an output of an A/D conversion means, This dynamic range control means is set up so that the response of dynamic range variable control operation according to an output of an A/D conversion means may become late, when operation of the data reproduction apparatus concerned is a stationary state, It is made to be set up so that the response of dynamic range variable control operation according to an output of an A/D conversion means may become early, when operation of the data reproduction apparatus concerned is in a special state. That is, while carrying out variable control of the dynamic range so that a dynamic range and an input signal level of an A/D conversion means may be in an always suitable state, The response of control is made late and priority is given to stability, and a response is made quick and it enables it to correspond to an amplitude change immediately in the special state where there is a possibility that a sudden amplitude change may occur, according to a stationary state considered that a sudden amplitude change hardly occurs.

[0023] As a dynamic range control means which can carry out variable control of the dynamic range in an A/D conversion means accommodative according to an output of an A/D conversion means, When performing control to which a dynamic range of an A/D conversion means is expanded, it carries out as [become / the response of dynamic range variable control operation according to an output of an A/D conversion means / early]. That is, top priority is given to a measure against overflow at the time of dynamic range expansion.

[0024] Prevention from saturation is realized about both A/D conversion processing and digital equalization processing by supervising both an output of an A/D conversion means, and an output of said equalization means, and establishing a dynamic range control means which can carry out variable control of the dynamic range in an A/D conversion means accommodative.

[0025]

[Embodiment of the Invention] Hereafter, the example realized as a DAT recording and reproducing device explains the data reproduction apparatus as various embodiments of this invention. Although this example digitizes voice data and uses it as record / DAT recording and reproducing device to reproduce, Even if it is a DAT system, a system by which other magnetic tape media are used, a magnetic disk system, an optical magnetic disk system, and an optical disk system as data storage apparatus for computer data etc., this invention is applicable similarly.

[0026] [A 1st embodiment] Drawing 1 is a block diagram of the DAT recording and reproducing device which performs record/playback of the audio signal over magnetic tape. The analog voice signal recorded is inputted from the terminal 1, and is changed into digital data with A/D converter 2. And an error correction code is added for every predetermined data unit by the encode part 3 for error corrections, and the digital data as a format for record is generated. The 8-10 modulation process of this digital data is carried out by the eight to 10 modulation part 4, it is made into the signal for record, and is supplied to the recording amplifier 6 via PURIKODA 5. Since a direct-current (DC) ingredient is cut via the following rotary transformer 7 as a signal for this record here, 8-10 abnormal conditions which are DC-free numerals rules are adopted. PURIKODA 5 is PURIKODA for example, in class 1 partial response (PR (1, 1)).

[0027]The signal amplified with the recording amplifier 6 is supplied to the recording head 8 in a rotating drum via the rotary transformer 7, and magnetic-recording operation to the magnetic tape 90 it is running by the recording head 8 is performed. After the magnetic tape 90 has inclined in the height direction to the rotating drum which carries the recording head 8 although not illustrated, it runs, being twisted and the rotating drum of a necessary angle degree is rotating ****ing to the magnetic tape 90, The recording track what is called by a helical scan is formed.

[0028]At the time of playback, the playback head 9 carried in the rotating drum traces the recording track because a rotating drum rotates while the magnetic tape 90 twisted around the rotating drum runs, and the recorded data is read. Although it is only that the playback head 9 of one recording head [8 or 1] is shown, a drawing top, Since an azimuth solid recording method is adopted actually, two recording heads and two playback heads from which an azimuth angle differs will be arranged on the peripheral surface of a rotating drum in the state where the predetermined angle separated mutually, respectively. When the head only for [of two] record and the head only for [of two] reproduction are used as a actual gestalt and two record reproduction heads are used, one record reproduction head, one recording head each, and a playback head may be adopted.

[0029]The signal read by the playback head 9 is supplied to the playback amplifier 11 via the rotary transformer 10. The rotary transformer 7 for record and the rotary transformer 10 for reproduction may be able to be actually made to serve a double purpose with one rotary transformer. Equalization processing of the signal amplified with the playback amplifier 11 is carried out in the analog equalizing circuit 12, and it is supplied to PLL circuit 13 and A/D converter 14. The analog equalizing circuit 12 is provided with the following.

The integration circuit which has an integration characteristic to low-pass [for amending the differentiation characteristic which it is constituted as what is called a common analog equalizer, and the playback head 9 has].

The differentiation circuit which has the differentiation characteristic to the high region for amending the loss by the gap of the playback head 9, etc.

The low pass filter which passes only the signal of a required zone.

The phase equalizer to which a phase is changed without changing amplitude in order to amend the circumference of the phase by this low pass filter.

[0030]PLL circuit 13 generates reproduction clock CK in sync with the output from the analog equalizing circuit 12, and supplies it as an operation clock to A/D converter 14, the digital equalizing circuit 15, the binarization circuit 16, the 10-8 converter 17, and the error correction part 18.

[0031]After the output from the analog equalizing circuit 12 is digital-data-ized with A/D converter 14, the signal (sample data SD) is inputted into the digital equalizing circuit 15. This digital equalizing circuit 15 is formed from a transversal filter and an adaptive equalization coefficient calculation circuit. And an adaptive equalization coefficient calculation circuit carries out variable generating of the tap coefficient accommodative according to the prediction error predicted from the output of a transversal filter, and controls filtering processing of a transversal filter. Although the work which minimizes the equalization error which remains in the signal of the output stage story of the analog equalizing circuit 12 will be performed in a transversal filter, the equalization characteristic for it will be set as an optimum state accommodative with the tap coefficient given from an adaptive equalization coefficient calculation circuit.

[0032]The signal by which filtering processing was carried out in the digital equalizing circuit 15 is supplied to the binarization circuit 16. In the binarization circuit 16, the signal inputted is binary-ized and it outputs to the 10-8 converter 17. In this example, the PRML method shall be adopted, the transfer characteristic from PURIKODA 5 to the output of the digital equalizing circuit 15 shall be made into a partial response characteristic, and, as for the binarization circuit 16, Viterbi decoding shall be performed.

[0033]The 10-8 converter 17 performs decode operation to eight to 10 abnormal conditions at the time of record. The decoded data is made into an analog signal with D/A converter 25, after

error correction processing is carried out in the error correction part 18. That is, it is considered as an analog voice signal from the first. And it is amplified with the amplifier 26 and outputted as a sound from the loudspeaker 27.

[0034] Sample data SD which is an output of A/D converter 14 is supplied also to the dynamic range control circuit 19. Although mentioned later in detail, the dynamic range control circuit 19 generates the value which sets the dynamic range of A/D converter 14 to sample data SD according to the various signals from the control signal generating section 21. Although the value is made into an analog voltage value with D/A converter 20, the analog voltage value serves as the reference voltage Vref of A/D converter 14. That is, A/D converter 14 is that reference voltage is changed by the dynamic range control circuit 19, and the dynamic range of A/D conversion operation will be changed. And operation as typically shown in drawing 2 by the dynamic range control circuit 19 performing feedback control based on the value of sample data SD which is an output of A/D converter 14 is realized.

[0035] Drawing 2 (a) is a case where RF signal amplitude is a large level comparatively, and it is that reference voltage Vref is made into a large value, and a dynamic range can extend when such, Let A/D converter 14 be a suitable dynamic range which is provided with a moderate saturation margin to an input signal and with which a quantization error will also become small. When RF signal amplitude becomes small like drawing 2 (b), it is that reference voltage Vref is made into a small value, and a dynamic range is made small, and A/D converter 14 is provided with a moderate saturation margin to an input signal, and let it be a suitable dynamic range also with a small quantization error.

[0036] Although the dynamic range control circuit 19 performs such dynamic range variable control fundamentally, especially as an example of a 1st embodiment, optimal dynamic range variable control is performed according to the various signals from the control signal generating section 21.

[0037] The various signals generated from the control signal generating section 21 are as follows. The timing reference signal TR is a signal used as the standard of the detection timing of sample data SD, for example, it is preferred for it to use the switching pulse (SWP) in sync with the head switching of the playback head 9 of the couple which serves as a reverse azimuth mutually, etc. as the timing reference signal TR.

[0038] The stationary state desired value M1 is a desired value for setting up a dynamic range comparatively small as a standard dynamic range. The special state target values M2 are desired values for setting up the comparatively large dynamic range as a standard dynamic range.

[0039] Special state detection signal SS is taken as the signal set to "H" from the search operation and operational mode transition time in a prescribed period. That is, the period which is performing the rapid-traverse search or the rewinding search about playback of the magnetic tape 90 is set to "H." With the time of operational mode transition, a reproduction → stop, reproduction → record, a reproduction → rapid-traverse search, Reproduction → A rewinding search, a stop → rapid-traverse search, a stop → rewinding search, Record → reproduction, a record → rapid-traverse search, record → it rewinds, and after a search etc. say the thing at the time of all change of operational mode and such operational mode change generates them, as for a prescribed period, special state detection signal SS is set to "H." That it is in change and the search state of operational mode detects the control signal generating section 21 with the signal from the system controller (microcomputer) which is not illustrated, for example, and a circuit system which sets special state detection signal SS to "H" by it should just be formed. Or naturally it is also possible to operate the system controller itself as the control signal generating section 21.

[0040] It detects that reproduction motion rushed into the existing recording part from the non-recording part on the magnetic tape 90, or that reproduction motion rushed into the non-recording part from the existing recording part on the magnetic tape 90 from an RF signal state, and may be made to set special state detection signal SS to "H" also in that case.

[0041] By the way, as a dashed line shows drawing 1, the output of the digital equalizing circuit 15 is also supplied to the dynamic range control circuit 19, but this serves as composition in case a 4th and 5th embodiment mentioned later is adopted.

[0042] Drawing 3 shows the important section of the example of the book as a 1st embodiment. The dynamic range control circuit 19 comprises the rectification circuit 31, the peak detection circuit 32, the timing generation part 33, the subtractor 34, the low pass filter 35, the multiplier 36, and the switch 37.

[0043] Sample data SD from A/D converter 14 is rectified in the rectification circuit 31. The situation of the rectifying operation of drawing 4 (a) and (b) is shown. When A/D converter 14 is an 8-bit A/D converter, for example, sample data SD can take the value from a positive value to a negative value like drawing 4 (a), it serves as 8 bit data. That is, as a quantized value of sample data SD, it is distributed to $-128 \sim +127$. It is rectified in the rectification circuit 31 (absolute-value-izing), and this sample data SD serves as data of only a positive value like drawing 4 (b).

[0044] Rectified sample data SDS is supplied to the peak detection circuit 32. The peak detection circuit 32 comprises the 51 or 8 bits of comparator flip-flop 52, and the switch 53 like drawing 5. A clear signal is supplied to the 8-bit flip-flop 52 from the timing generation part 33. Clock CK from PLL circuit 13 is supplied as a latch clock. Rectified sample data SDS is supplied to the comparator 51 and Ti terminal of the switch 53.

[0045] The comparator 51 compares size about the latch output of sample data SDS and the flip-flop 52 which are inputted, and controls the switch 53 by the comparison result. That is, only when sample data SDS is larger, the switch 53 is connected to Ti terminal, and sample data SDS is stored up in the flip-flop 52. The value which connects the switch 53 to To terminal when the latch output of the flip-flop 52 is larger than sample data SDS, therefore is accumulated in the flip-flop 52 is maintained as it is. The latch output of the flip-flop 52 serves as peak detection value PK.

[0046] This peak detection operation becomes like drawing 4 (c) – (e). The timing generation part 33 generates the clear signal CLR like drawing 4 (d) to the flip-flop 52 according to the timing reference signal TR like drawing 4 (c). The flip-flop 52 is cleared by this clear signal CLR, and the latch output of the flip-flop 52 is measured from sample data SDS from that time. Since the accumulation value of the flip-flop 52 is updated if sample data SDS is larger, peak detection value PK becomes like drawing 4 (e). When the clear signal CLR is generated by one track of the reproduction motion on the magnetic tape 90 to 1 time of timing, peak detection value PK is obtained by 1 track unit.

[0047] Peak detection value PK is supplied to the subtractor 34, and the desired value M is subtracted. And the error E, i.e., the difference of a peak value and the desired value M, acquired by the subtraction is supplied to the low pass filter 35. As the low pass filter 35 is shown in drawing 4 (f) from the timing generation part 33, clock (LPF clock) CK_L is supplied rather than

the clear signal to the timing which carried out prescribed period delay, and smooth operation is performed based on this LPF clock CK_L . That is, the error E in the timing from which peak detection value PK of the flip-flop 52 became a peak value in 1 track correctly serves as a candidate for data smoothing. And in the low pass filter 35, smoothing is performed for the error E inputted between the errors E about a part for a neighboring track, i.e., the number track of the past, the multiplication of the coefficient alpha will be carried out with the multiplier 36, and the smoothed signal EAV will be outputted to D/A converter 20.

[0048] As a result of such a series of operations, when peak detection value PK is smaller than the desired value M, the output value to D/A converter 20 becomes small, and thereby, the dynamic range of A/D converter 14 is corrected in the direction which becomes small. Conversely, if peak detection value PK is larger than the desired value M, the dynamic range of A/D converter 14 will be corrected in the direction which becomes large.

[0049] When sample data SD shall take the value of $-128 \sim +127$ here, I think that M was set as the desired value +110. Then, it will be controlled for the peak value of sample data SD of a one track period to average in this case, and to be set to ± 110 . In this case, the surplus ratio to the saturation in A/D converter 14 is $\{(127-110) / 110\} \times 100 = 15$ (%).

It comes out.

[0050] What is necessary is on the other hand, just to make the desired value M small for the increase in a quantization error, when [a certain] thinking that he would like to increase a

saturation surplus ratio, even if it carries out grade permission. For example, it is set as the desired value $M+50$. Since the dynamic range of A/D converter 14 at this time will change in the direction which becomes large to the input signal amplitude to A/D converter 14, a saturation surplus ratio increases. Namely, $\{(127-50)/50\} \times 100 = 154\%$. It becomes. That is, it will not be saturated until the input to A/D converter 14 large-amplitude-izes 2.54 times suddenly.

[0051] When there is a possibility that large amplitude-ization [**** / as an input from the above thing to A/D converter 14] may occur, it is understood that what is necessary is to make the value of the desired value M small and just to make a saturation margin high. So, in this example, the control signal generating section 21 supplies two values, the stationary state desired value $M1$ and the special state target values $M2$, to 37Tswitch 1 terminal and T2 terminal as a value which can be used as the desired value M , respectively. The stationary state desired value $M1$ sets up a comparatively small dynamic range, and is made into the value for lessening a quantization error, for example, is made into $M1 = "110"$. The special state target values $M2$ are desired values for setting up a dynamic range comparatively large even if it carries out grade permission, in order [a certain] to enlarge a saturation margin, for example, the increase in a quantization error is made into $M2 = "50"$.

[0052] And the control signal generating section 21 supplies special state detection signal SS set to "H" from the search operation and operational mode transition time in a prescribed period to the dynamic range control circuit 19 as a switching control signal of the switch 37, as mentioned above. If special state detection signal SS is set to "H", T2 terminal will be connected to the switch 37, and as for the switch 37, T1 terminal will be connected if special state detection signal SS is set to "L".

[0053] It is the period when special state detection signal SS is "L" at the usual reproduction motion time (stationary state), and the stationary state desired value $M1$ is supplied to the subtractor 34 as the desired value M at this time. Therefore, when $M1 = "110"$, as mentioned above, a saturation surplus ratio is 15% and the dynamic range of A/D converter 14 will be controlled to an input signal by the suitable state with few quantization errors. On the other hand, in a prescribed period, a (special state) and the special state target values $M2$ are supplied to the subtractor 34 as the desired value M from the period, at i.e., the search operation and operational mode transition time, when special state detection signal SS is "H." Therefore, if $M1 = "50"$, as mentioned above, a saturation surplus ratio is 154%, and as for the dynamic range of A/D converter 14, although a quantization error is large, it will be controlled to an input signal by the state where it had sufficient saturation margin.

[0054] The situation of dynamic range control is typically shown in drawing 6. Suppose that operational mode changed to the time base direction (at the $t1 - t6$ time) with the stop \rightarrow reproduction \rightarrow rapid-traverse (FF) search \rightarrow rewind (REW) search \rightarrow reproduction \rightarrow stop. Drawing 6 (a) shows change of the desired value M , and drawing 6 (b) shows change of a saturation surplus ratio.

[0055] After reproduction is first started from a halt condition, since special state detection signal SS is set to "H", the special state target values $M2$ are used as the desired value M , fixed time's ($t0-t1$) dynamic range is large, that is, a large saturation margin is taken at it. If it goes through predetermined time and special state detection signal SS is set to "L" ($t1-t3$), the stationary state desired value $M1$ is used as the desired value M , and although a dynamic range is small and a saturation margin is small, it will change a quantization error into a small state.

[0056] If it shifts to a rapid-traverse search from $t2$ time, special state detection signal SS will be set to "H", a dynamic range will be enlarged, and, as for the rewind search at the $t3 - t4$ time, this state will be continued. Even if it furthermore shifts to reproduction motion at the $t4$ time, till $t5$ point in time which is a prescribed period from mode change, special state detection signal SS is still "H", and the state where the dynamic range was enlarged is continued. and $t5$ time or subsequent ones -- $t6$ time -- until -- it changes a dynamic range into the small state where a quantization error is small, as a stationary state.

[0057] Namely, in this example, an input signal makes the dynamic range of A/D converter 14 small according to a certain stationary state which is carrying out grade stability, Aim at

- improvement in an error rate by lessening a quantization error, and on the other hand, when there is a possibility of causing change with a sudden input signal to A/D converter 14, the time of a search and mode change, etc., Even if a certain grade permits a quantization error, the dynamic range of A/D converter 14 is enlarged and an error is prevented from increasing to a degree very much by taking sufficient saturation margin so that the situation of overflow which must be avoided most may not occur.

[0058][A 2nd embodiment] Drawing 7 and drawing 8 explain the example as a 2nd embodiment. The composition as [whole] a recording and reproducing device presupposes that it is the same as that of drawing 1, and only an important section is shown in drawing 7.

[0059]A different point from the dynamic range control circuit 19 in a 1st embodiment of the above in the dynamic range control circuit 19 in this example, It is the point of performing operation by which there is no switch 37, the fixed desired value's M being supplied to the subtractor 34 from the control signal generating section 21 and special state detection signal SS are inputted into the low pass filter 35, and special state detection signal SS controls the response time constant of the low pass filter 35.

[0060]Although the low pass filter 35 is formed as for example, an IIR digital filter, the common model of an IIR digital filter is shown in drawing 8 (a). That is, the multiplication of the input data is carried out to the coefficient K with the multiplier 71, and via the adding machine 72, it is delayed 1 sample timing and outputted in the delay circuit 73. The multiplication of the output of the delay circuit 73 is carried out to a coefficient (1-K) with the multiplier 74 again, and it is fed back to the adding machine 72. It is known for such an IIR digital filter that a response time constant will change with the values of the coefficient K (and 1-K).

[0061]So, in this example, the speed of response of a dynamic range control loop is changed by making it change the value of the coefficient K (and 1-K) based on special state detection signal SS.

[0062]The period when special state detection signal SS is "L" is at the usual reproduction motion time (stationary state), as mentioned above, and an amplitude change rapid as an input of A/D converter 14 at this time does not appear. and -- in order to raise the stability of a dynamic range control loop -- the response as the dynamic range control circuit 19 -- a certain grade -- it is better to make it late. Then, the low pass filter 35 sets the period when special state detection signal SS is "L", for example to coefficient $K = 0.1$ and coefficient $(1-K) = 0.9$. then, the response time constant of the low pass filter 35 -- drawing 8 (b) -- like -- a certain grade -- it changes into a late state.

[0063]On the other hand, in a prescribed period, a (special state) and an amplitude change rapid as an input of A/D converter 14 may arise from the period, at i.e., the search operation and operational mode transition time, when special state detection signal SS is "H." In such a case, it is necessary to react immediately as dynamic range control operation, and to avoid overflow and increase of a quantization error. Then, the low pass filter 35 sets the period when special state detection signal SS is "H", for example to coefficient $K = 0.3$ and coefficient $(1-K) = 0.7$, and changes a response time constant into a quick state like drawing 8 (c).

[0064]In such this example, answer immediately [when an amplitude change rapid as an input of A/D converter 14 arises in the time of a search, etc.], and the dynamic range of A/D converter 14 is changed properly, Overflow and increase of a quantization error can be avoided and, on the other hand, always [constant], a late response can realize stability of a dynamic range control loop moderately.

[0065][A 3rd embodiment] Drawing 9 explains the example as a 3rd embodiment. The composition as [whole] a recording and reproducing device presupposes that it is the same as that of drawing 1, and only an important section is shown in drawing 9. A different point from the example as a 2nd embodiment which this example mentioned above is a point of having formed the positive/negative evaluating part 38. About the value of the error E which is an output of the subtractor 34, the positive/negative evaluating part 38 distinguishes a positive value or a negative value, and supplies it to the low pass filter 35 by making the discriminated result into the time number change signal J.

[0066]As operation of the dynamic range control 19, When the error E is a negative value when

peak detection value PK is smaller than the desired value M namely, as mentioned above, It controls so that the dynamic range of A/D converter 14 becomes small, and on the other hand, when the error E is a positive value when peak detection value PK is larger than the desired value M namely, it controls so that the dynamic range of A/D converter 14 becomes large. The positive/negative evaluating part 38 distinguishes whether the present processing controls by positive/negative judgment of the error E to become small about whether it controls so that a dynamic range becomes large. And the damping time constant of the low pass filter 35 will be controlled by the discriminated result.

[0067]drawing 8 (b) which the low pass filter 35 set, for example to coefficient $K = 0.1$ and coefficient $(1-K) = 0.9$, and was mentioned above when it was distinguished that the error E is negative -- like -- the response time constant of the low pass filter 35 -- a certain grade -- it changes into a late state. On the other hand, when it is distinguished that the error E is positive, it is made for the low pass filter 35 to set to coefficient $K = 0.3$ and coefficient $(1-K) = 0.7$, and it changes a response time constant into a quick state like drawing 8 (c).

[0068]That is, in the dynamic range control circuit 19 of this example, when expanding the dynamic range of A/D converter 14, a response is made quick. The time of expanding a dynamic range is a time of the input signal amplitude to A/D converter 14 becoming large, that is, is a time of a possibility that overflow will arise occurring. Therefore, when such, it is performing expansion control of a dynamic range by a quick response, and overflow generating is prevented. That is, it can be said that it is what strengthens the preventing function to the overflow which must not take place most.

[0069][A 4th embodiment] The important section of a 4th embodiment is shown in drawing 10. It is the point which he is trying to supervise also about the output of the digital equalizing circuit 15 as a feature of the dynamic range control circuit 19 in this example as the dashed line showed also to drawing 1. In this example, sample data SD which is an output of A/D converter 14 is inputted into the rectification circuit 31A, and is set to sample data SDS1 rectified. The output of the digital equalizing circuit 15 is inputted into the rectification circuit 31B, and is set to data SDS2 rectified similarly.

[0070]Sample data SDS1 rectified in the rectification circuit 31A is supplied to TS1 terminal and the comparator 39 of the switch 40. Data SDS2 rectified in the rectification circuit 31B is supplied to TS2 terminal and the comparator 39 of the switch 40.

[0071]The comparator 39 performs size comparison about the value of data SDS1 inputted and SDS2, and outputs the comparison result as a control signal over the switch 40. That is, if data SDS1 is larger, terminal TS1 will be connected to the switch 40, and if data SDS2 is larger, terminal TS2 will be connected to the switch 40.

[0072]Therefore, the data of the larger one as an absolute value among the outputs of sample data SD outputted from A/D converter 14 and the digital equalizing circuit 15 will be supplied to the peak detection circuit 32, and will be made into the object of peak detection operation. And like each example mentioned above, peak detection value PK and the desired value M are subtracted with the subtractor 34, and variable control of a dynamic range is performed according to the acquired error E.

[0073]In such this example, the digital equalizing circuit 15 will also be included in a dynamic range control loop. Even if overflow does not occur in A/D converter 14, there will also be a possibility that sample data may overflow by the operation in the digital equalizing circuit 15. What is necessary is just to enlarge the dynamic range of A/D converter 14, when there is such fear in order to prevent the overflow in the digital equalizing circuit 15.

[0074]By then, the thing for which the digital equalizing circuit 15 is also included in a dynamic range control loop like this example, both the output of the digital equalizing circuit 15 and the output of A/D converter 14 are supervised, and peak detection is performed. The dynamic range control of A/D converter 14 kept from generating the overflow in the digital equalizing circuit 15 is attained.

[0075][A 5th embodiment] The important section of a 4th embodiment is shown in drawing 11. This example is provided with all the features of the 1st explained so far -- the dynamic range control circuit as a 4th embodiment.

[0076] That is, like a 1st embodiment, it is made for the switch 37 to switch according to special state detection signal SS, that is, the desired value M is switched to the stationary state desired value M1 and the special state target values M2 by special state detection signal SS. Thereby, in a regular reproduction state, few, at the time of a search, a dynamic range is enlarged at the time of mode transition, and a saturation margin is acquired [with a small dynamic range] also to a sudden large amplitude input the time in a quantization error.

[0077] Like a 2nd embodiment, while changing the response time constant of the low pass filter 35 by special state detection signal SS, even if it responds to positive/negative evaluation of the error E like a 3rd embodiment, the response time constant of the low pass filter 35 is changed. For this reason, special state detection signal SS is supplied to the low pass filter 35 via OR gate 41, and the damping time constant change signal J from the positive/negative evaluating part 38 is supplied to the low pass filter 35 via OR gate 41.

[0078] Therefore, at the time of a search, at the time of mode transition, it changes the low pass filter 35 into a high speed response state, and also when it carries out expansion control of the dynamic range further, it changes it into a high speed response state. Even if an amplitude change rapid as an input of A/D converter 14 arises by this, answer immediately and the dynamic range of A/D converter 14 is changed properly, A response is made quick so that overflow and increase of a quantization error can be avoided, and on the other hand, always [constant], the stability of a dynamic range control loop is moderately obtained as a late response. It enables it to avoid overflow certainly by changing into a high speed response state also at the time of the dynamic range expansion with fear of overflow.

[0079] Since he is trying to incorporate the output of the digital equalizing circuit 15 as well as [still] a 4th embodiment into a dynamic range control loop, not only A/D converter 14 but the function of the prevention from overflow in the digital equalizing circuit 15 will be exhibited.

[0080]

[Effect of the Invention] As explained above, in the data reproduction apparatus of this invention. It is considered as the dynamic range control means which can carry out variable control of the dynamic range in an A/D conversion means, When operation of the data reproduction apparatus concerned is a stationary state, it is small in a dynamic range, and it is made to control to enlarge a dynamic range, when operation of the data reproduction apparatus concerned is in a special state. For this reason, while variable control is carried out, a dynamic range, so that the dynamic range and input signal level of an A/D conversion means may be in an always suitable state, In the stationary state considered that a sudden amplitude change hardly occurs, the dynamic range of an A/D conversion means is made small, a quantization error is made small, and improvement in the error rate as regenerative data can be realized. In the special state where there is a possibility that a sudden amplitude change may occur, a dynamic range is enlarged, a saturation margin is enlarged, preventing overflow at least is realized, and it is effective in the ability to prevent an error from increasing to a degree very much. The effect will be most demonstrated for using the time of being especially in a special state with the period when the data reproduction apparatus concerned is performing the search operation, and a prescribed period when operational mode changes effectively.

[0081] A dynamic range control means is set up so that the response of the dynamic range variable control operation according to the output of the A/D conversion means may become late, when operation of the data reproduction apparatus concerned is a stationary state, It is setting up so that the response of the dynamic range variable control operation according to the output of the A/D conversion means may become early, when operation of the data reproduction apparatus concerned is in a special state, When a rapid amplitude change arises in a special state, it can answer immediately and a dynamic range can be changed properly, and overflow and increase of a quantization error can be avoided. It is effective in the stability of a dynamic range control loop being moderately realizable with a late response at the time of regular. The effect is most demonstrated effectively by using the time of being in a special state also about this with the period when the data reproduction apparatus concerned is performing the search operation, and a prescribed period when operational mode changes.

[0082] Furthermore, by this invention, when performing control to which the dynamic range of an

A/D conversion means is expanded, the dynamic range control means is made to be set up so that the response of the dynamic range variable control operation according to the output of the A/D conversion means may become early. That is, it is effective in the ability to strengthen the preventing function to the overflow which must not take place most with making a response quick at the time of expansion control of the dynamic range which a possibility that overflow will arise generates.

[0083] Since he is trying to have a dynamic range control means which supervises both the output of an A/D conversion means, and the output of an equalization means, and can furthermore carry out variable control of the dynamic range in an A/D conversion means accommodative in this invention, It is effective in control keep overflow from generating being realized about both an A/D conversion means and an equalization means.

[0084] And from the above effects, as a data reproduction apparatus of this invention, Stability of improvement in the reproduction performance of apparatus and search performance and the control loop at the time of regular, etc. are realized by improvement in the error rate at the time of stationary operation, the prevention from error rate aggravation by the prevention from saturation in an A/D conversion means and an equalization means, and improvement in the speed of until control-loop stable. For this reason, there are circuitry to add and an effect that it is realizable by being simple.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention]This invention changes into digital data the signal read from the recording medium, performs equalization processing and decoding, and relates to the data reproduction apparatus which reproduces data.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a block diagram of the recording and reproducing device of an embodiment of the invention.

[Drawing 2]It is an explanatory view of the fundamental dynamic range control action of an embodiment.

[Drawing 3]It is a block diagram of the important section of a 1st embodiment.

[Drawing 4]It is an explanatory view of operation of the dynamic range control circuit of an embodiment.

[Drawing 5]It is a circuit diagram of the peak detection circuit of an embodiment.

[Drawing 6]It is an explanatory view of dynamic range control operation of an embodiment.

[Drawing 7]It is a block diagram of the important section of a 2nd embodiment.

[Drawing 8]It is an explanatory view of the response of the low pass filter of an embodiment.

[Drawing 9]It is a block diagram of the important section of a 3rd embodiment.

[Drawing 10]It is a block diagram of the important section of a 4th embodiment.

[Drawing 11]It is a block diagram of the important section of a 5th embodiment.

[Drawing 12]It is an explanatory view of the eye pattern of a partial-response-equalization waveform.

[Drawing 13]It is an explanatory view of the distribution state of sampling data.

[Drawing 14]It is an explanatory view of a proper dynamic range established state.

[Drawing 15]Compared with a dynamic range, it is an explanatory view of the state where an input signal level is low.

[Drawing 16]Compared with a dynamic range, it is an explanatory view of the distribution state of the sampling data in the state where an input signal level is low.

[Drawing 17]Compared with a dynamic range, it is an explanatory view of the distribution state of the sampling data in the state where an input signal level is low.

[Drawing 18]Compared with a dynamic range, it is an explanatory view of the distribution state of the sampling data in the state where an input signal level is lower.

[Drawing 19]Compared with a dynamic range, it is an explanatory view of the distribution state of the sampling data in the state where an input signal level is lower.

[Drawing 20]Compared with a dynamic range, an input signal level is an explanatory view of the distribution state of the sampling data in a state very low to a degree.

[Drawing 21]Compared with a dynamic range, an input signal level is an explanatory view of the distribution state of the sampling data in a state very low to a degree.

[Drawing 22]Compared with a dynamic range, it is an explanatory view of the distribution state of the sampling data in the state where an input signal level is large.

[Drawing 23]Compared with a dynamic range, it is an explanatory view of the state where an input signal level is large.

[Drawing 24]Compared with a dynamic range, it is an explanatory view of the distribution state of the sampling data in the state where an input signal level is still larger.

[Drawing 25]Compared with a dynamic range, it is an explanatory view of the state where an input signal level is still larger.

• [Description of Notations]

- 4 8 -10 modulation part and 5 PURIKODA, 6 recording amplifier, and 7 and 10 Rotary encoder, 8 A recording head, 9 playback heads, 11 playback amplifier, and 12 Analog equalizing circuit, 13 A PLL circuit, 14 A/D converters, and 15 Digital equalizing circuit, 16 A binarization circuit and 17 10-8 converter, 18 error correction parts, 19 dynamic range control circuit, 20 A D/A converter and 21 [A subtractor and 35 / A low pass filter and 36 / A switch and 38 / A positive/negative evaluating part and 39 / A comparator and 41 / OR gate] A multiplier, and 37 and 40 A control signal generating section, and 31, 31A and 31B A rectification circuit, 32 peak detection circuits, 33 timing generation parts, and 34

[Translation done.]

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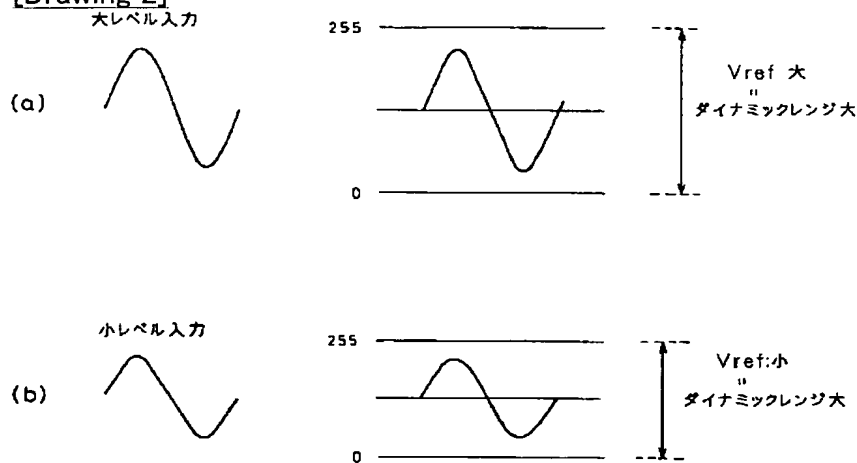
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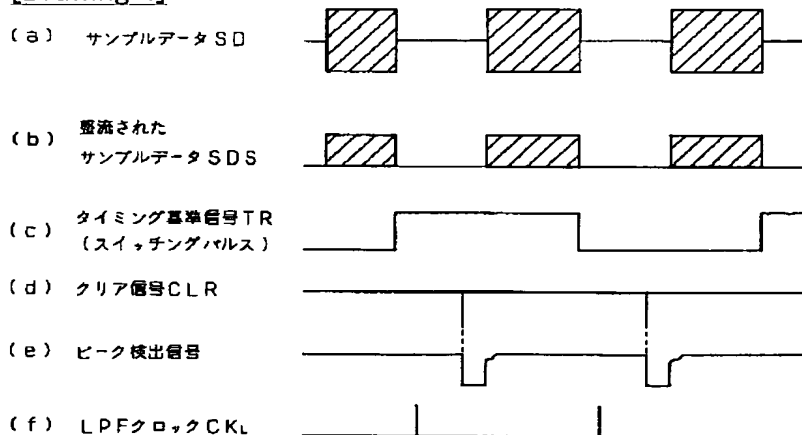
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DRAWINGS

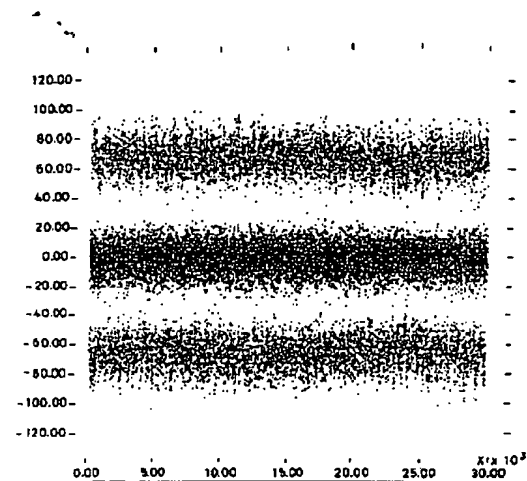
[Drawing 2]



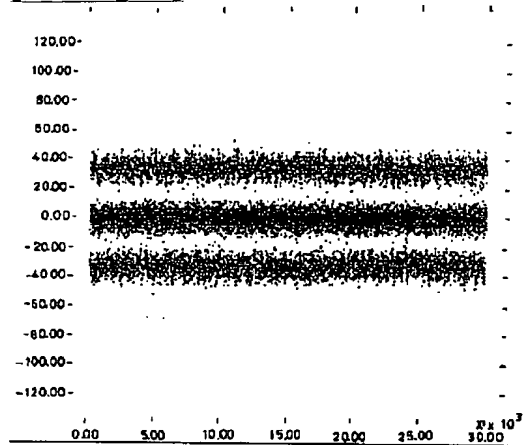
[Drawing 4]



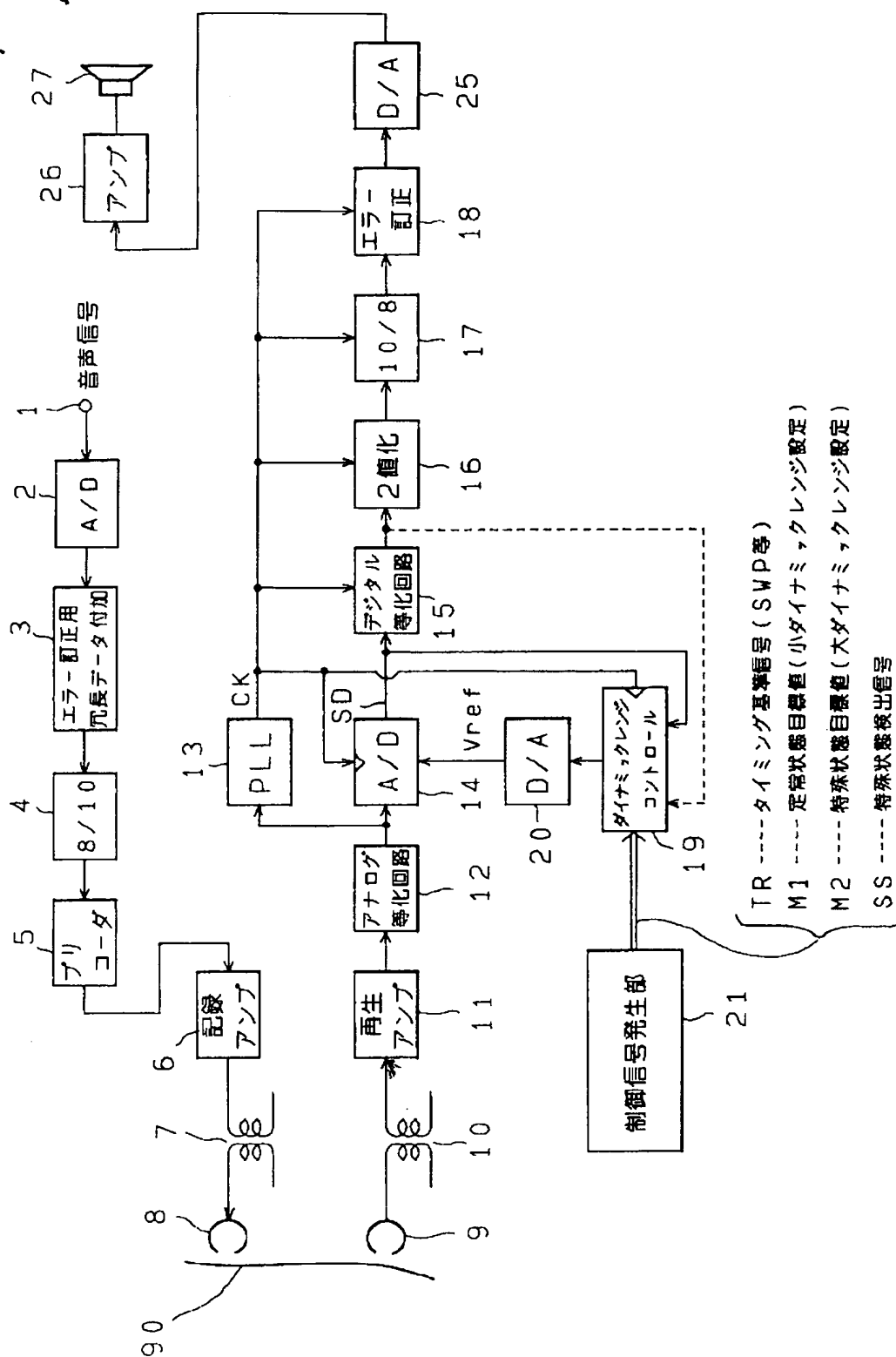
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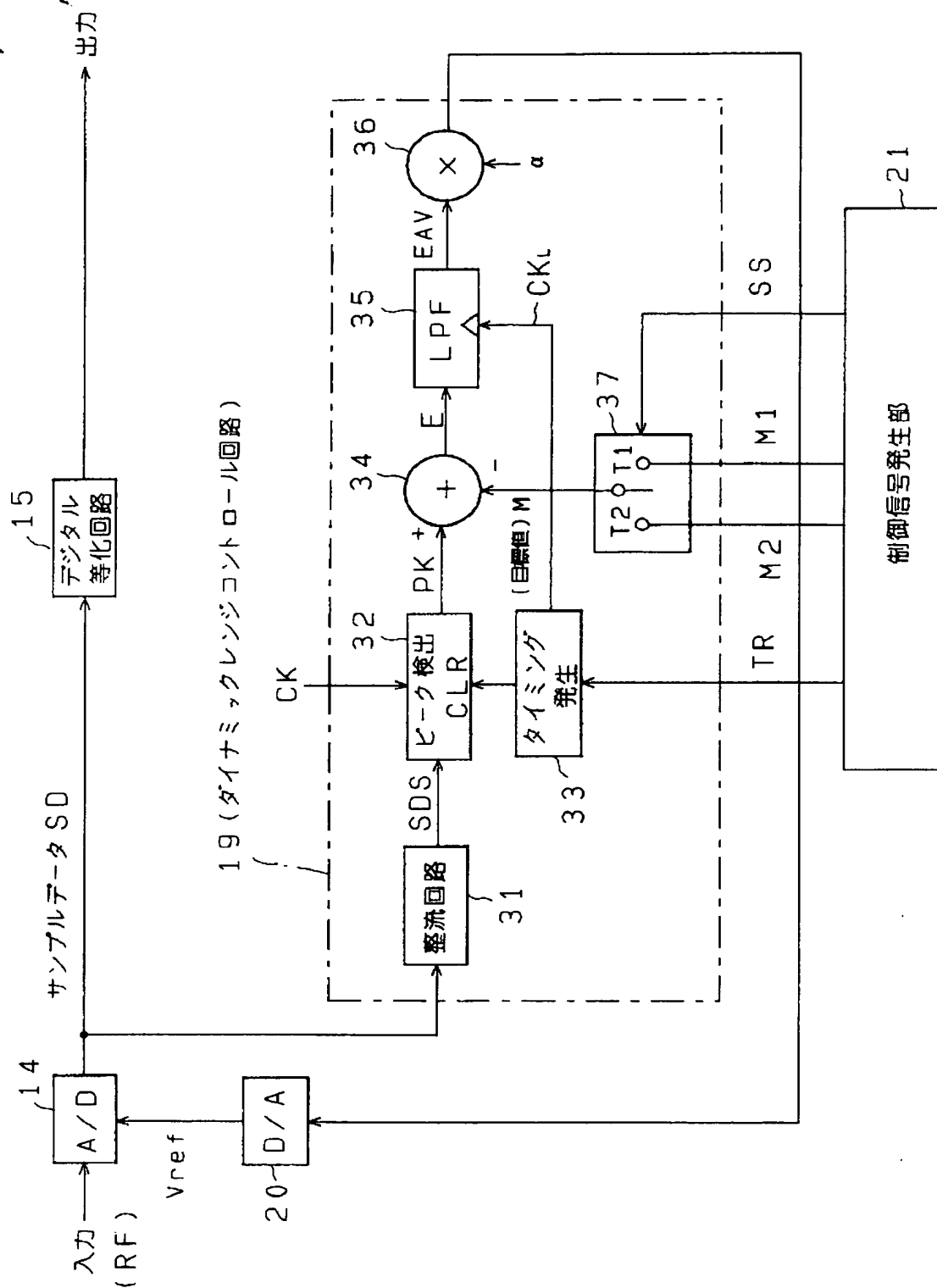
[Drawing 16]



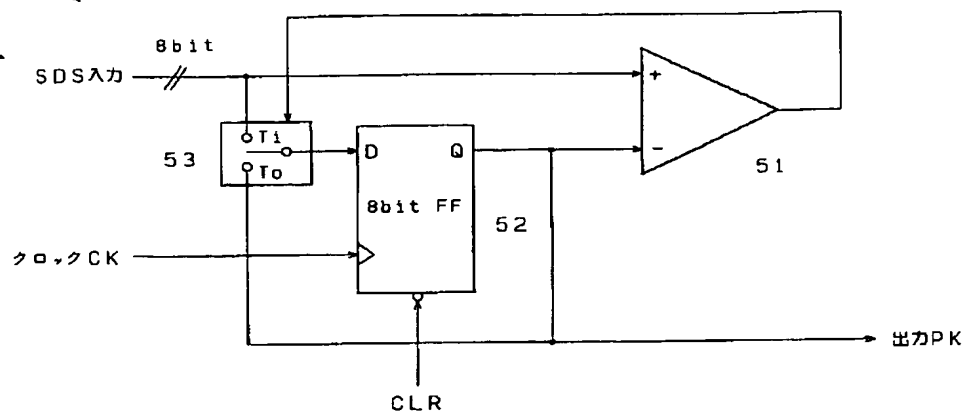
[Drawing 1]



[Drawing 3]



[Drawing 5]

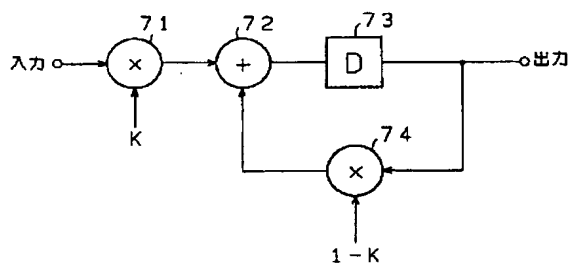


ピーク検出回路 32

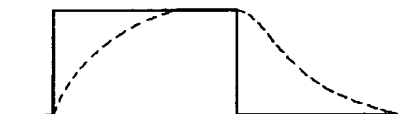
[Drawing 8]

IIRフィルタのモデル (LPF 35)

(a)

(b) $K=0.1$, $1-K=0.9$

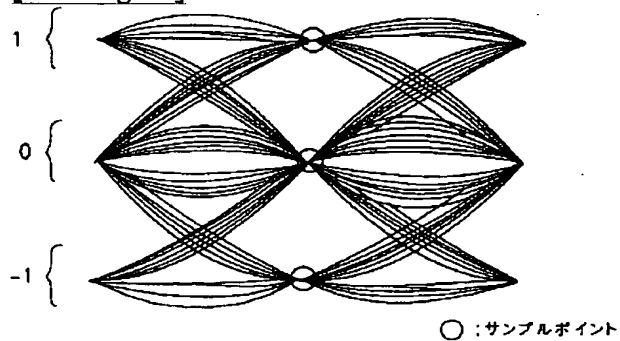
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(c) $K=0.3$, $1-K=0.7$

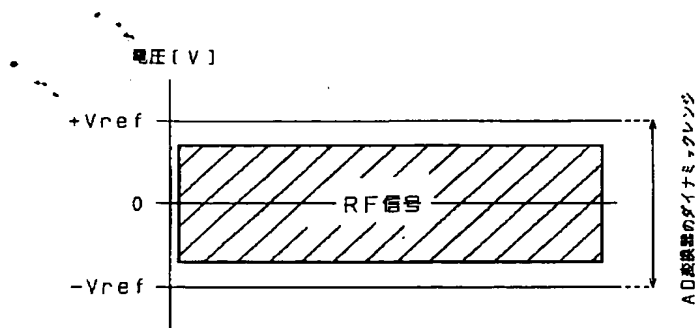
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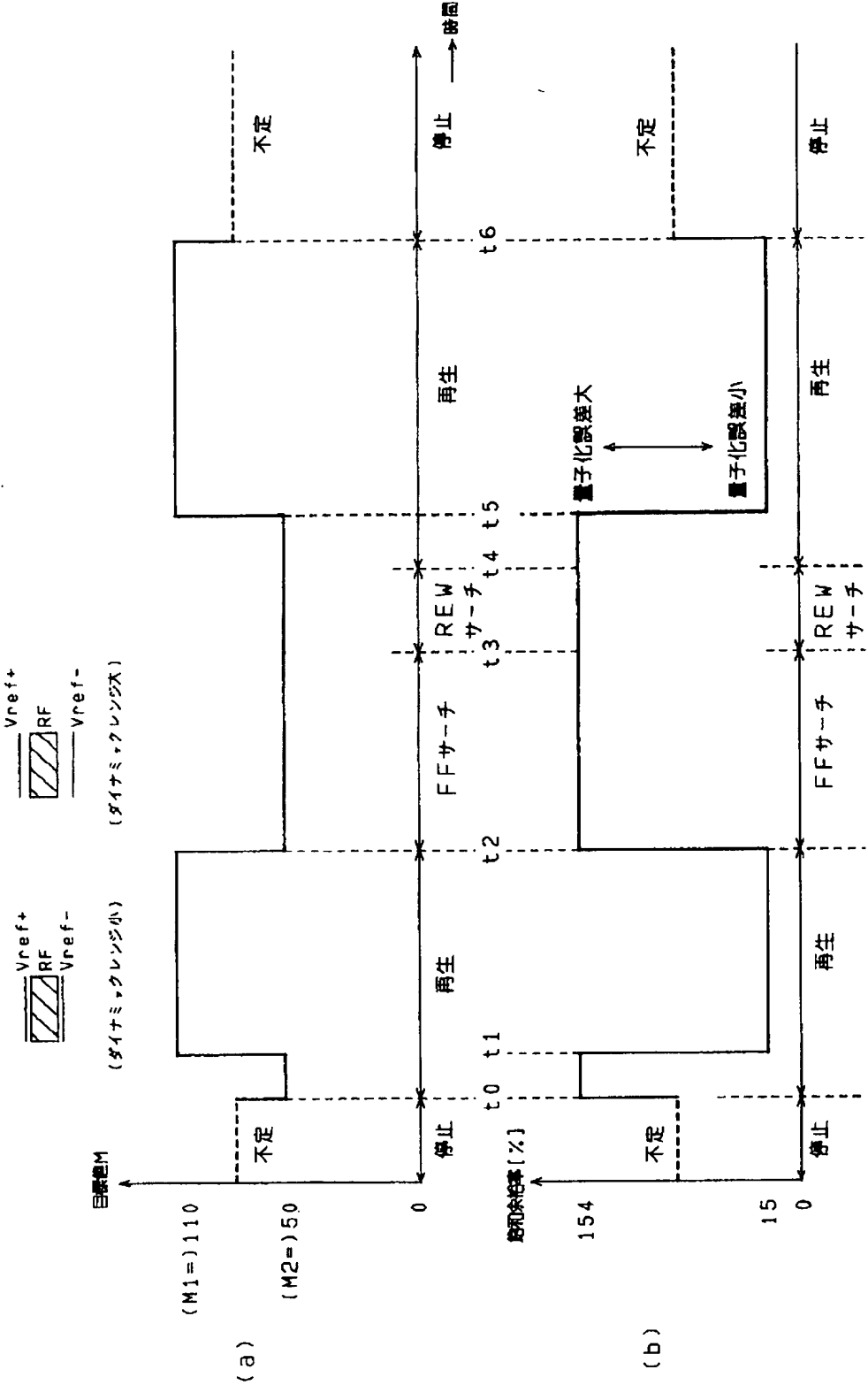
[Drawing 12]



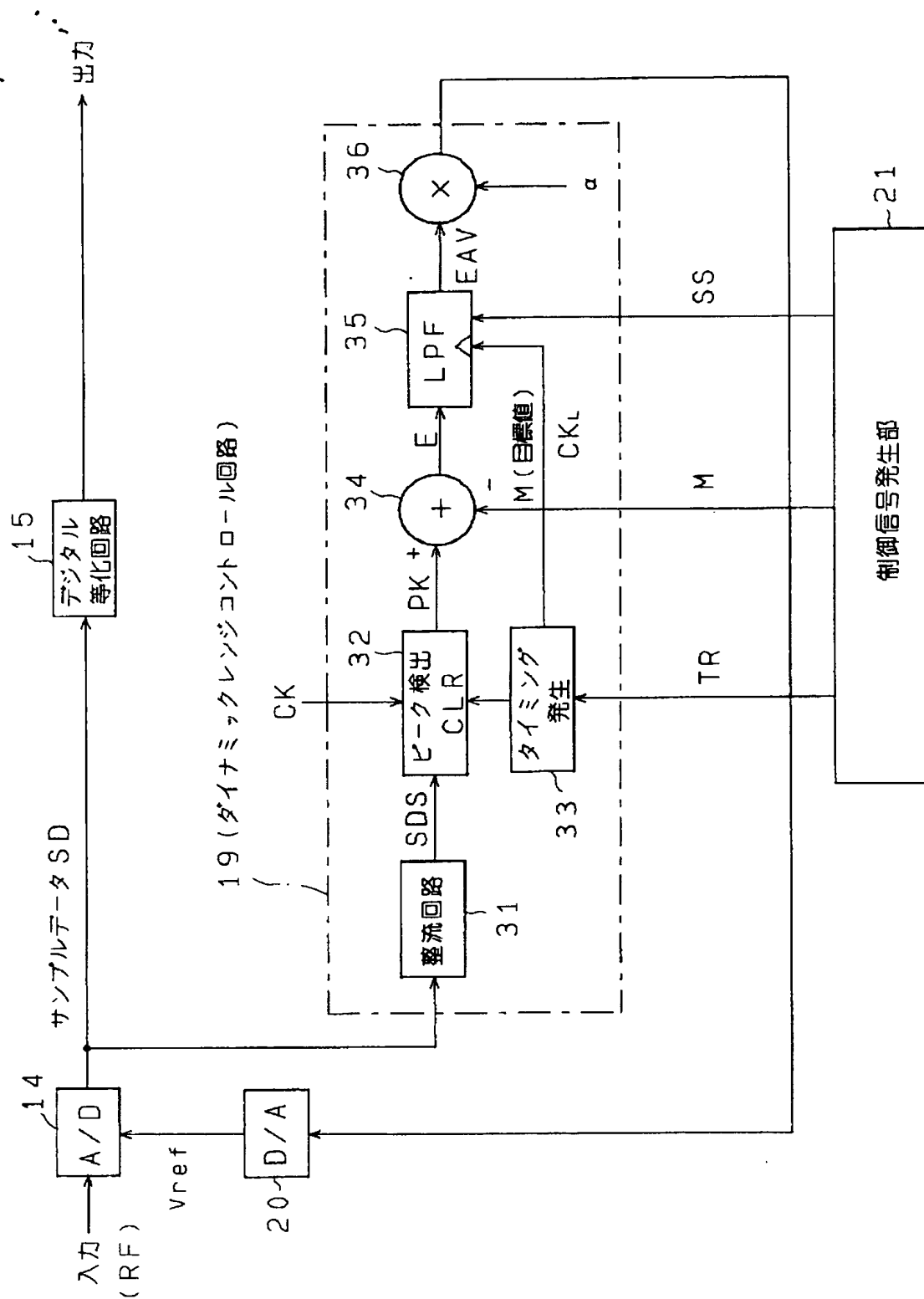
[Drawing 14]



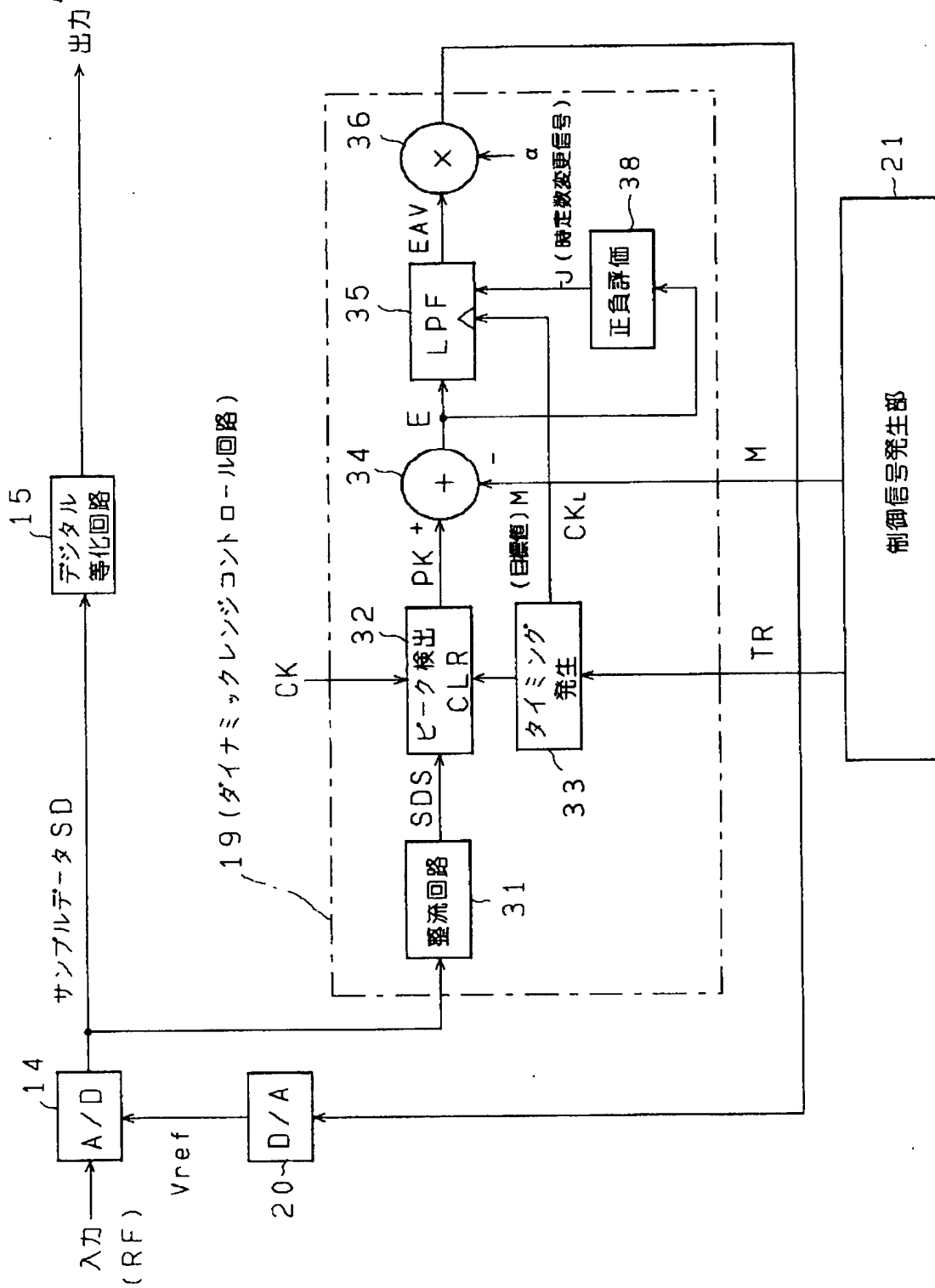
[Drawing 6]



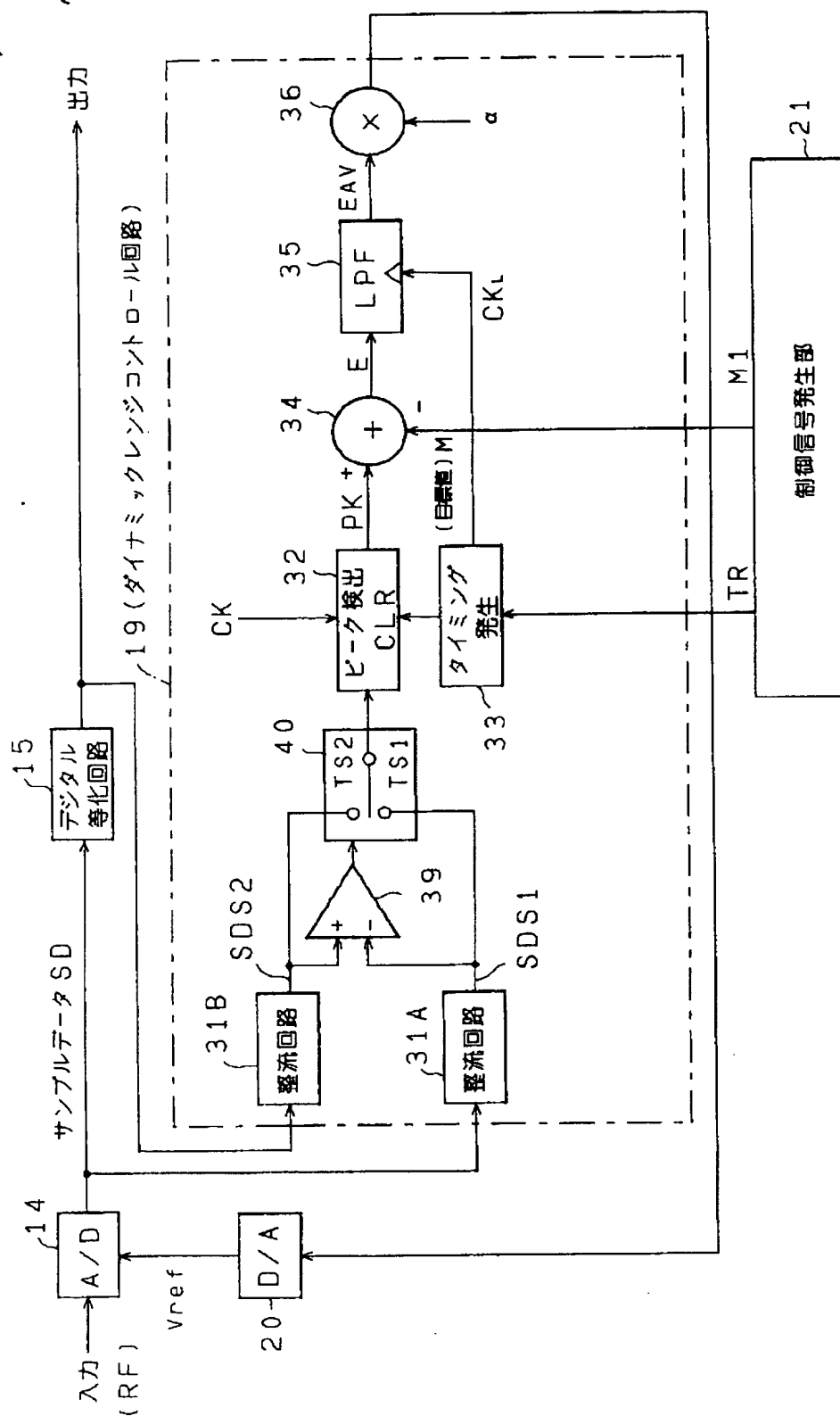
[Drawing 7]



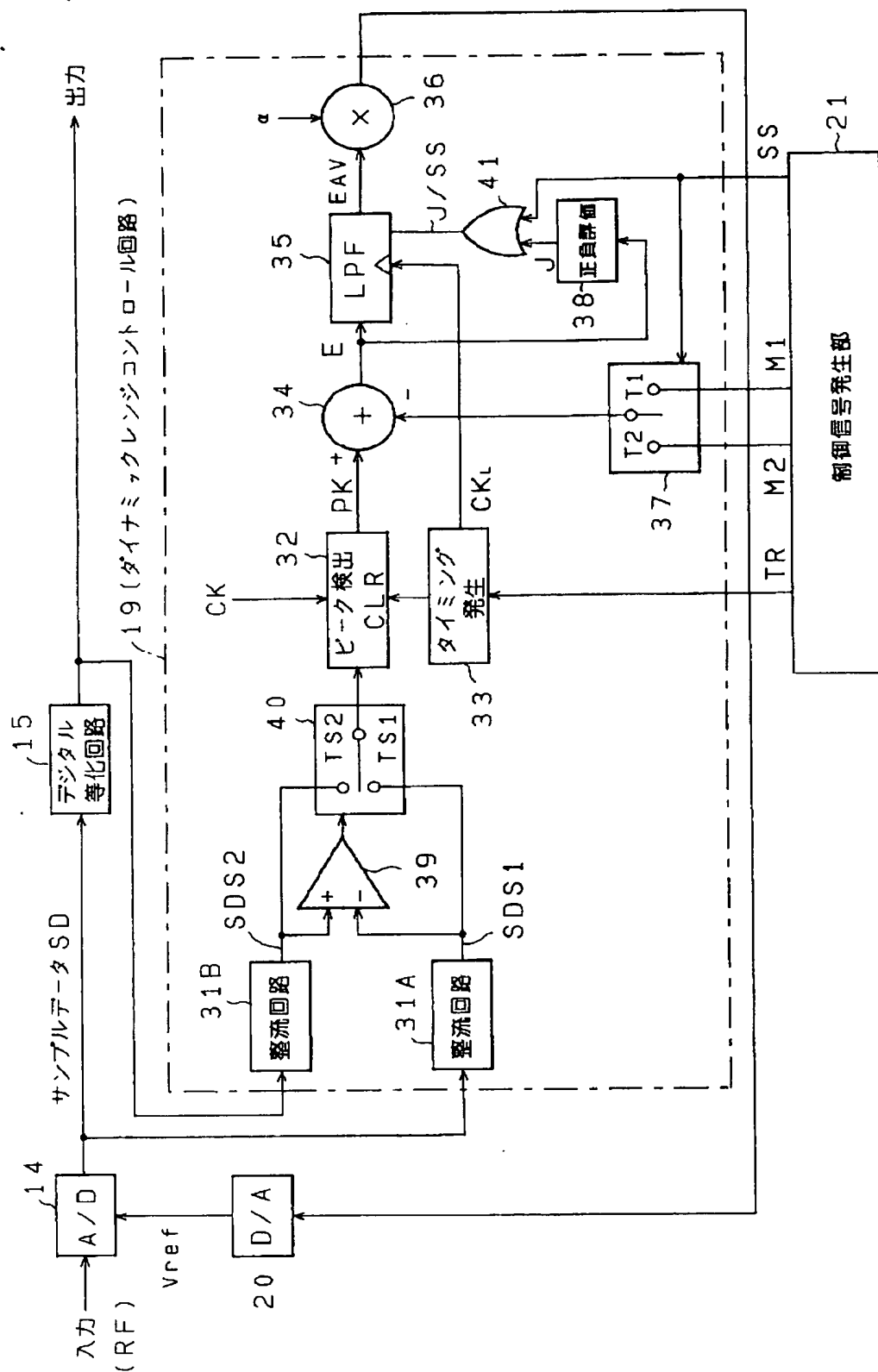
[Drawing 9]



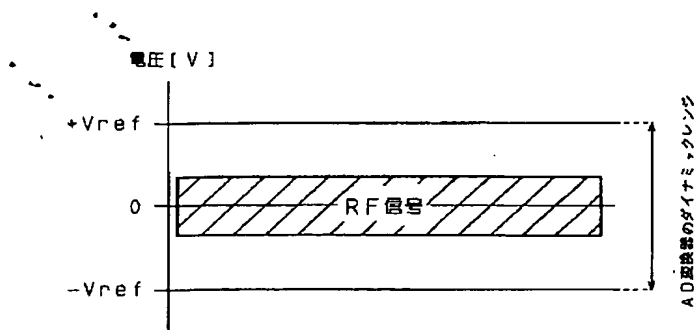
[Drawing 10]



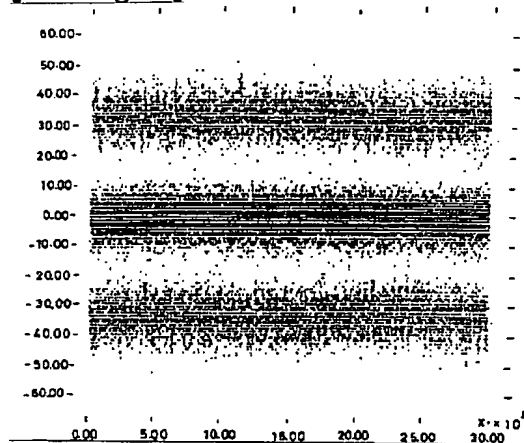
[Drawing 11]



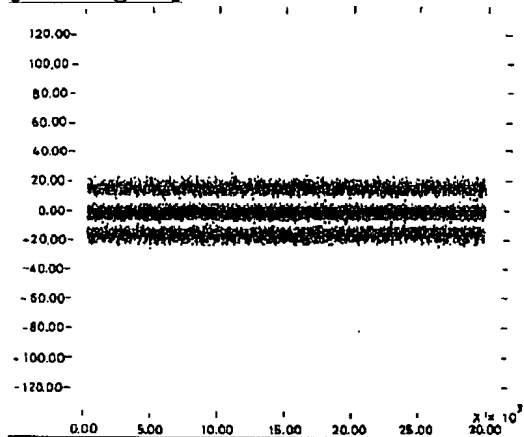
[Drawing 15]



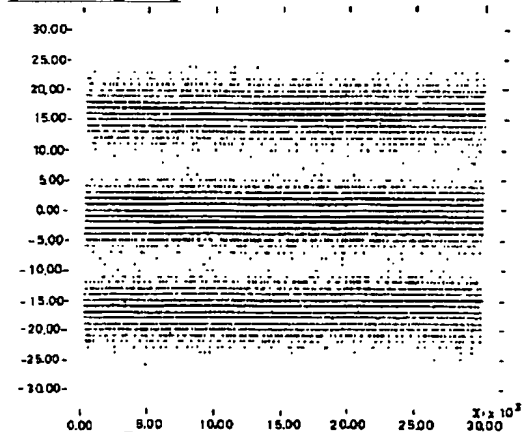
[Drawing 17]



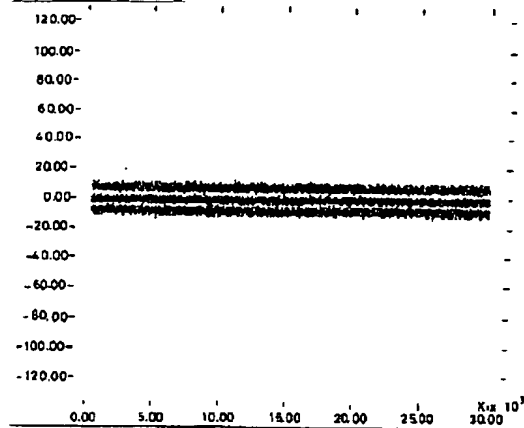
[Drawing 18]



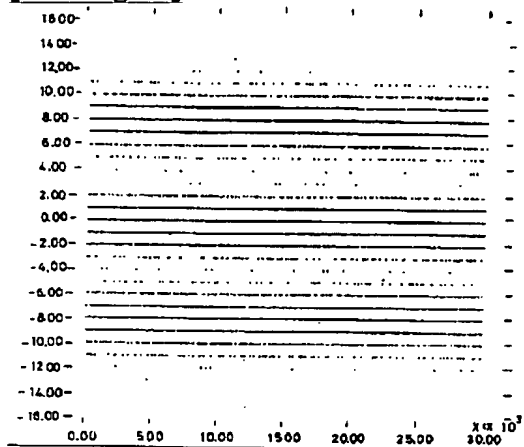
[Drawing 19]



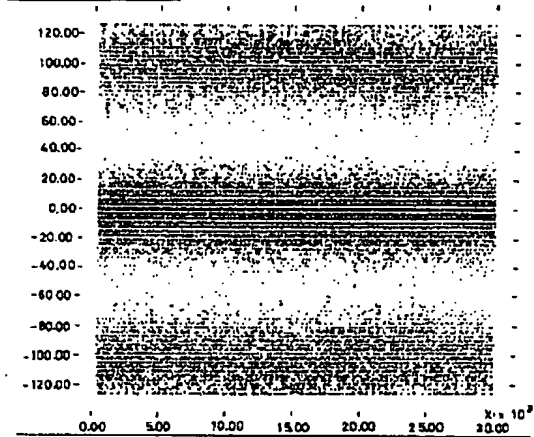
[Drawing 20]



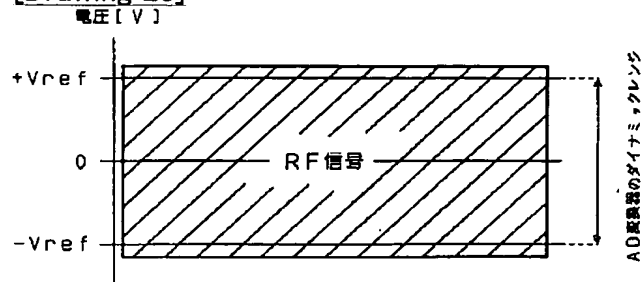
[Drawing 21]



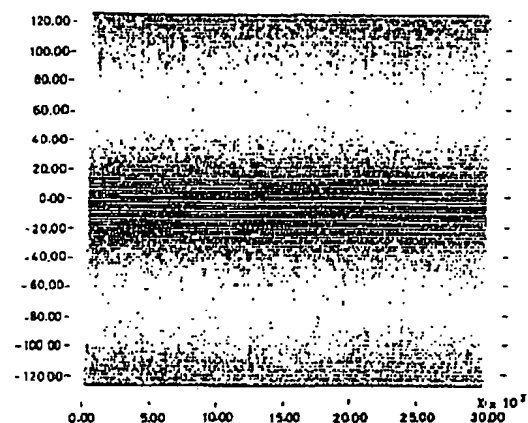
[Drawing 22]



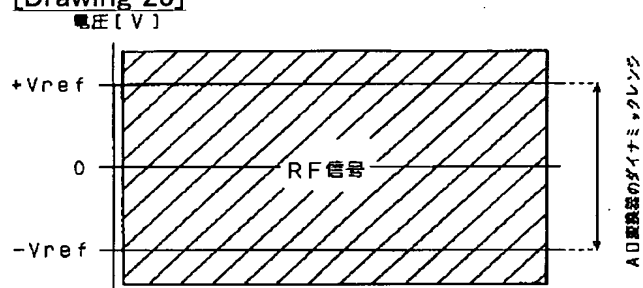
[Drawing 23]



[Drawing 24]



[Drawing 25]



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- 3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art]Various kinds of recording media, such as magnetic tape, a magnetic disk, an optical disc, and a magneto-optical disc, and the recording and reproducing device corresponding to it have spread. In the playback equipment in a high-density digital recording system in recent years, the A/D conversion of a deed and the RF signal by which equalization was carried out is carried out for the equalization processing by the analog equalizer or a digital filter to the signal (RF signal) read from the recording medium by the playback head. And equalization processing, binarization processing, decoding, error correction processing, etc. are performed to digital data, and data is reproduced in many cases. This an equalization method as RF signal treatment technique of a high-density digital recording system A partial response method, It is because the example which adopts the combination (PRML method) of a maximum likelihood decoding method (Viterbi decoding: Viterbi detection : Maximum Likelyhood Detection Method) for a detection system is increasing.

[0003]For example, performed binary-ization, when the DAT (digital audio tape) recording and reproducing device was mentioned as the example, as RF processing, by the analog limiting circuit, old adopted integration equalization, are easy composition of decoding and an error correction, and were ending, but. Since the Viterbi detecting operation is the structure which binary-izes the detecting point voltage system sequence (sampling-data series) of the RF signal by which equalization was carried out by carrying out digital signal processing when a PRML method is adopted, the A/D converter for sampling an RF signal is needed.

[0004]However, it has a dynamic range peculiar as a signal input range in which an analog to digital is possible, when an input signal level is not an appropriate range compared with a dynamic range, good sample data is not obtained, but the situation where detection errors occur frequently produces an A/D converter.

[0005]That is, when the RF signal of remarkable small amplitude is inputted compared with a dynamic range, the quantization error under output (sample data) of an A/D converter increases, and since the signal to noise ratio gets worse, a detection error increases. When the RF signal of large amplitude which exceeds a dynamic range is inputted, sample data will turn into saturated data, namely, the linearity in A/D conversion operation will be spoiled. The signal to noise ratio of such sample data has deteriorated in the degree very much, and a detection error increases substantially.

[0006]Drawing 12 - drawing 25 explain these situations. An RF signal is explained that it is the waveform by which equalization was carried out by the class 1 partial-response method (PR (1, 1) method). Drawing 12 is an eye pattern of a class 1 partial-response-equalization waveform. This equalization waveform can take three kinds of values, "1", "0", and "-1", with the sample point (detecting point) shown by O in a figure. However, since an actual waveform contains a noise, as shown in this figure, it does not converge on one point with a sample point, and it varies.

[0007]A sampling of such a waveform will acquire the sample data distribution distributed focusing on three voltage like drawing 13. In a 30000-point table, this drawing 13 is the shown graph about the sample data value (pressure value) which sampled the RF signal with the A/D converter. This is in a state as shown the dynamic range of an A/D converter in the schematic

diagram 14, when the accuracy of an A/D converter is 8 bits (-128 to $+127$) and it sets up. That is, it is a case where it is assumed that the saturation margin of a certain grade is taken as a dynamic range of an A/D converter to the amplitude (slash part) of an RF signal waveform like drawing 14, and the dynamic range of an A/D converter is generally set as a proper state to RF signal amplitude. In such a case, sampling-data distribution of about 2^{100} points was acquired like drawing 13.

[0008]Next, the case where RF signal voltage (amplitude) becomes half mostly like drawing 15 compared with drawing 14 is considered. The sample data distribution at this time becomes like drawing 16. The same scale as said drawing 13 shows the graph of drawing 16, and drawing 17 expanded this. Sample data distribution turns into distribution of the range of about 2^{50} points, especially sample data distribution is sparse so that drawing 17 may be compared and understood to drawing 13, so that drawing 16 may show. This means that the quantization error is increasing because RF signal amplitude becomes small to the dynamic range of an A/D converter.

[0009]Distribution when RF signal voltage (amplitude) becomes about $1/4$, and the abbreviation $1/8$ compared with the state of drawing 14 is shown in drawing 18 and drawing 20, respectively. The same scale as said drawing 13 shows drawing 18 and drawing 20, and that to which having expanded drawing 18 expanded drawing 19 and drawing 20 is drawing 21. From these figures, it is understood that a quantization error increases, so that it is observed that sample data distribution is still more sparse, that is, RF signal amplitude becomes small to the dynamic range of an A/D converter.

[0010]Next, the case where it becomes the thing that RF signal amplitude exceeds the dynamic range of an A/D converter is considered. Drawing 22 shows distribution of the sample data at the time of setting up the dynamic range of an A/D converter, as shown in drawing 23. That is, compared with the case where the dynamic range is standard like drawing 14, RF signal amplitude is an example used as about 1.5 time. In the distribution state of drawing 22, the maximum of the value of sample data is restricted to $+127$, the minimum is restricted to -128 , and being saturated is observed. RF signal voltage is only about 1.5. Although becoming change which double size hears was only carried out, the linearity of A/D conversion operation is spoiled by this. And normal operation of the Viterbi decoding will not be carried out to such a sample data series, but errors will occur frequently.

[0011]Furthermore, drawing 24 shows distribution of the sample data at the time of setting up the dynamic range of an A/D converter, as shown in drawing 25. This is the example from which RF signal amplitude became twice [about] compared with the case where the dynamic range is standard like drawing 14. The maximum of the value of sample data having been restricted to $+127$, and the minimum having been restricted to -128 , and being saturated also with the distribution state of this drawing 24 is observed. And when RF signal voltage becomes large twice [about], the linearity of A/D conversion operation will be spoiled greatly, and normal operation of the Viterbi decoding will not be carried out to such a sample data series, but errors will occur frequently more.

[0012]When an input signal level is not an appropriate range compared with a dynamic range as mentioned above, good sample data will not be obtained from an A/D converter, but detection errors will occur frequently. These people performed the proposal indicated to Japanese Patent Application No. No. 183945 [six to] as advanced technology to such a situation. The art which uses an input signal as a suitable level to the dynamic range of an A/D converter by establishing the AGC circuit (automatic gain control circuit) which controls the input level of an A/D converter according to the output of an A/D converter in this Japanese Patent Application No. No. 183945 [six to] is indicated.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, in the data reproduction apparatus of this invention. It is considered as the dynamic range control means which can carry out variable control of the dynamic range in an A/D conversion means, When operation of the data reproduction apparatus concerned is a stationary state, it is small in a dynamic range, and it is made to control to enlarge a dynamic range, when operation of the data reproduction apparatus concerned is in a special state. For this reason, while variable control is carried out, a dynamic range, so that the dynamic range and input signal level of an A/D conversion means may be in an always suitable state, In the stationary state considered that a sudden amplitude change hardly occurs, the dynamic range of an A/D conversion means is made small, a quantization error is made small, and improvement in the error rate as regenerative data can be realized. In the special state where there is a possibility that a sudden amplitude change may occur, a dynamic range is enlarged, a saturation margin is enlarged, preventing overflow at least is realized, and it is effective in the ability to prevent an error from increasing to a degree very much. The effect will be most demonstrated for using the time of being especially in a special state with the period when the data reproduction apparatus concerned is performing the search operation, and a prescribed period when operational mode changes effectively.

[0081]A dynamic range control means is set up so that the response of the dynamic range variable control operation according to the output of the A/D conversion means may become late, when operation of the data reproduction apparatus concerned is a stationary state, It is setting up so that the response of the dynamic range variable control operation according to the output of the A/D conversion means may become early, when operation of the data reproduction apparatus concerned is in a special state, When a rapid amplitude change arises in a special state, it can answer immediately and a dynamic range can be changed properly, and overflow and increase of a quantization error can be avoided. It is effective in the stability of a dynamic range control loop being moderately realizable with a late response at the time of regular. The effect is most demonstrated effectively by using the time of being in a special state also about this with the period when the data reproduction apparatus concerned is performing the search operation, and a prescribed period when operational mode changes.

[0082]Furthermore, by this invention, when performing control to which the dynamic range of an A/D conversion means is expanded, the dynamic range control means is made to be set up so that the response of the dynamic range variable control operation according to the output of the A/D conversion means may become early. That is, it is effective in the ability to strengthen the preventing function to the overflow which must not take place most with making a response quick at the time of expansion control of the dynamic range which a possibility that overflow will arise generates.

[0083]Since he is trying to have a dynamic range control means which supervises both the output of an A/D conversion means, and the output of an equalization means, and can furthermore carry out variable control of the dynamic range in an A/D conversion means accommodative in this invention, It is effective in control keep overflow from generating being realized about both an A/D conversion means and an equalization means.

[0084]And from the above effects, as a data reproduction apparatus of this invention, Stability of

improvement in the reproduction performance of apparatus and search performance and the control loop at the time of regular, etc. are realized by improvement in the error rate at the time of stationary operation, the prevention from error rate aggravation by the prevention from saturation in an A/D conversion means and an equalization means, and improvement in the speed of until control-loop stable. For this reason, there are circuitry to add and an effect that it is realizable by being simple.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]The following problems are left behind although the input signal level to the dynamic range of an A/D converter can usually be made into an appropriate range by providing the AGC circuit to the input signal of an A/D converter.

[0014]In playback equipment, when operational modes, such as reproduction motion and a search operation, change, reproduction motion rushes into an existing recording part from the non-recording part on a recording medium, and reproduction motion rushes into a non-recording part from the existing recording part on a recording medium, an RF signal level may be changed sharply.

[0015]Although it is required also for the sudden amplitude increase which is produced as the dynamic range of the A/D converter mentioned above, and a relation of an input signal level in such a case to make management possible, it is required to set up a dynamic range more greatly beforehand for the purpose. That is, it is giving a saturation margin. However, in such a case, it is also that a quantization error increases. That is, two requirements of [usually follow only by the input level control at the time, and] reduction in a quantization error and the correspondence to sudden large amplitude by an AGC circuit cannot be satisfied.

[0016]If the response performance of an AGC circuit is considered about the time of sudden change of input signal amplitude, the following problems will arise. Since AGC control is carried out so that a small level signal may be in a proper state to the dynamic range of an A/D converter till then when RF signal amplitude changes from a small level to a large level suddenly first, at the time of a sudden large amplitude input, a dynamic range will become [too little] relatively. Therefore, since sample data is saturated by the period until an AGC circuit lowers a gain to a proper state corresponding to a large amplitude input, the signal to noise ratio deteriorates greatly and an error increases it to a degree very much. Therefore, an AGC circuit is asked for quick response performance so that it can answer immediately at large amplitude in such a case.

[0017]Since it is in the state where the dynamic range is adapted for the large amplitude RF signal till then when RF signal amplitude changes from a large level to a small level suddenly, a dynamic range will become excessive relatively to a small level input. For this reason, a quantization error increases and degradation of the signal to noise ratio and increase of an error arise also in this case. Therefore, an AGC circuit is asked for quick response performance also in this case.

[0018]However, if speed of response is sped up, convergency will worsen and an AGC loop will become unstable. For this reason, high speed response-ization was not able to be performed, so that it could respond to the sudden amplitude change enough. And in the apparatus to which operational modes, such as reproduction/search, change from the difficult situation of high-speed-response-izing frequently like computer data storage apparatus, it became disadvantageous especially. That is, it is because an overhead until an AGC circuit is stabilized becomes long and the reaction velocity of apparatus becomes slow by this.

[0019]Considering the device furthermore provided with the digital equalizing circuit, even if sample data is not saturated with the output stage story of an A/D converter, there is a possibility that overflow may arise to data by the operation of a digital equalizing circuit. Since

change of an equalization characteristic cannot be predicted in the case of the apparatus which adjusts especially an equalization characteristic automatically (adaptive equalization), supervising also about the output signal of an equalizing circuit is called for.

[Translation done.]

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MEANS

[Means for Solving the Problem]While this invention presupposes that it is controllable so that a dynamic range and an input signal level of an A/D conversion means may be in an always suitable state in view of the above problems, conflicting requirements of making small enlarging a dynamic range of an A/D conversion means and acquiring a saturation margin, and a quantization error -- a case -- a division -- being able to be satisfied -- making -- things. opposite requirements of the stability of a control loop, and improvement in the speed of speed of response -- a case -- a division -- being able to be satisfied -- making -- things. When required, in performing giving priority to a measure against saturation over a measure against a quantization error, and digital equalization, it aims at realizing prevention from saturation in the digital equalization processing.

[0021]For this reason, have a dynamic range control means which can carry out variable control of the dynamic range in an A/D conversion means first, and this dynamic range control means, When operation of the data reproduction apparatus concerned is a stationary state, it is small in a dynamic range, and it controls to enlarge a dynamic range, when operation of the data reproduction apparatus concerned is in a special state. That is, while carrying out variable control of the dynamic range so that a dynamic range and an input signal level of an A/D conversion means may be in an always suitable state, Although a sudden amplitude change makes a dynamic range of an A/D conversion means small and makes a quantization error small in a stationary state considered to hardly generate, In the special state where there is a possibility that a sudden amplitude change may occur, a dynamic range is enlarged, a saturation margin is enlarged and overflow is prevented.

[0022]It has a dynamic range control means which can carry out variable control of the dynamic range in an A/D conversion means accommodative according to an output of an A/D conversion means, This dynamic range control means is set up so that the response of dynamic range variable control operation according to an output of an A/D conversion means may become late, when operation of the data reproduction apparatus concerned is a stationary state, It is made to be set up so that the response of dynamic range variable control operation according to an output of an A/D conversion means may become early, when operation of the data reproduction apparatus concerned is in a special state. That is, while carrying out variable control of the dynamic range so that a dynamic range and an input signal level of an A/D conversion means may be in an always suitable state, The response of control is made late and priority is given to stability, and a response is made quick and it enables it to correspond to an amplitude change immediately in the special state where there is a possibility that a sudden amplitude change may occur, according to a stationary state considered that a sudden amplitude change hardly occurs.

[0023]As a dynamic range control means which can carry out variable control of the dynamic range in an A/D conversion means accommodative according to an output of an A/D conversion means, When performing control to which a dynamic range of an A/D conversion means is expanded, it carries out as [become / the response of dynamic range variable control operation according to an output of an A/D conversion means / early]. That is, top priority is given to a measure against overflow at the time of dynamic range expansion.

[0024]Prevention from saturation is realized about both A/D conversion processing and digital

equalization processing by supervising both an output of an A/D conversion means, and an output of said equalization means, and establishing a dynamic range control means which can carry out variable control of the dynamic range in an A/D conversion means accommodative. [0025]

[Embodiment of the Invention] Hereafter, the example realized as a DAT recording and reproducing device explains the data reproduction apparatus as various embodiments of this invention. Although this example digitizes voice data and uses it as record / DAT recording and reproducing device to reproduce, Even if it is a DAT system, a system by which other magnetic tape media are used, a magnetic disk system, an optical magnetic disk system, and an optical disk system as data storage apparatus for computer data etc., this invention is applicable similarly.

[0026] [A 1st embodiment] Drawing 1 is a block diagram of the DAT recording and reproducing device which performs record/playback of the audio signal over magnetic tape. The analog voice signal recorded is inputted from the terminal 1, and is changed into digital data with A/D converter 2. And an error correction code is added for every predetermined data unit by the encode part 3 for error corrections, and the digital data as a format for record is generated. The 8-10 modulation process of this digital data is carried out by the eight to 10 modulation part 4, it is made into the signal for record, and is supplied to the recording amplifier 6 via PURIKODA 5. Since a direct-current (DC) ingredient is cut via the following rotary transformer 7 as a signal for this record here, 8-10 abnormal conditions which are DC-free numerals rules are adopted. PURIKODA 5 is PURIKODA for example, in class 1 partial response (PR (1, 1)).

[0027] The signal amplified with the recording amplifier 6 is supplied to the recording head 8 in a rotating drum via the rotary transformer 7, and magnetic-recording operation to the magnetic tape 90 it is running by the recording head 8 is performed. After the magnetic tape 90 has inclined in the height direction to the rotating drum which carries the recording head 8 although not illustrated, it runs, being twisted and the rotating drum of a necessary angle degree is rotating ***ing to the magnetic tape 90, The recording track what is called by a helical scan is formed.

[0028] At the time of playback, the playback head 9 carried in the rotating drum traces the recording track because a rotating drum rotates while the magnetic tape 90 twisted around the rotating drum runs, and the recorded data is read. Although it is only that the playback head 9 of one recording head [8 or 1] is shown, a drawing top, Since an azimuth solid recording method is adopted actually, two recording heads and two playback heads from which an azimuth angle differs will be arranged on the peripheral surface of a rotating drum in the state where the predetermined angle separated mutually, respectively. When the head only for [of two] record and the head only for [of two] reproduction are used as a actual gestalt and two record reproduction heads are used, one record reproduction head, one recording head each, and a playback head may be adopted.

[0029] The signal read by the playback head 9 is supplied to the playback amplifier 11 via the rotary transformer 10. The rotary transformer 7 for record and the rotary transformer 10 for reproduction may be able to be actually made to serve a double purpose with one rotary transformer. Equalization processing of the signal amplified with the playback amplifier 11 is carried out in the analog equalizing circuit 12, and it is supplied to PLL circuit 13 and A/D converter 14. The analog equalizing circuit 12 is provided with the following.

The integration circuit which has an integration characteristic to low-pass [for amending the differentiation characteristic which it is constituted as what is called a common analog equalizer, and the playback head 9 has].

The differentiation circuit which has the differentiation characteristic to the high region for amending the loss by the gap of the playback head 9, etc.

The low pass filter which passes only the signal of a required zone.

The phase equalizer to which a phase is changed without changing amplitude in order to amend the circumference of the phase by this low pass filter.

[0030] PLL circuit 13 generates reproduction clock CK in sync with the output from the analog

equalizing circuit 12, and supplies it as an operation clock to A/D converter 14, the digital equalizing circuit 15, the binarization circuit 16, the 10-8 converter 17, and the error correction part 18.

[0031] After the output from the analog equalizing circuit 12 is digital-data-ized with A/D converter 14, the signal (sample data SD) is inputted into the digital equalizing circuit 15. This digital equalizing circuit 15 is formed from a transversal filter and an adaptive equalization coefficient calculation circuit. And an adaptive equalization coefficient calculation circuit carries out variable generating of the tap coefficient accommodative according to the prediction error predicted from the output of a transversal filter, and controls filtering processing of a transversal filter. Although the work which minimizes the equalization error which remains in the signal of the output stage story of the analog equalizing circuit 12 will be performed in a transversal filter, the equalization characteristic for it will be set as an optimum state accommodative with the tap coefficient given from an adaptive equalization coefficient calculation circuit.

[0032] The signal by which filtering processing was carried out in the digital equalizing circuit 15 is supplied to the binarization circuit 16. In the binarization circuit 16, the signal inputted is binary-ized and it outputs to the 10-8 converter 17. In this example, the PRML method shall be adopted, the transfer characteristic from PURIKODA 5 to the output of the digital equalizing circuit 15 shall be made into a partial response characteristic, and, as for the binarization circuit 16, Viterbi decoding shall be performed.

[0033] The 10-8 converter 17 performs decode operation to eight to 10 abnormal conditions at the time of record. The decoded data is made into an analog signal with D/A converter 25, after error correction processing is carried out in the error correction part 18. That is, it is considered as an analog voice signal from the first. And it is amplified with the amplifier 26 and outputted as a sound from the loudspeaker 27.

[0034] Sample data SD which is an output of A/D converter 14 is supplied also to the dynamic range control circuit 19. Although mentioned later in detail, the dynamic range control circuit 19 generates the value which sets the dynamic range of A/D converter 14 to sample data SD according to the various signals from the control signal generating section 21. Although the value is made into an analog voltage value with D/A converter 20, the analog voltage value serves as the reference voltage V_{ref} of A/D converter 14. That is, A/D converter 14 is that reference voltage is changed by the dynamic range control circuit 19, and the dynamic range of A/D conversion operation will be changed. And operation as typically shown in drawing 2 by the dynamic range control circuit 19 performing feedback control based on the value of sample data SD which is an output of A/D converter 14 is realized.

[0035] Drawing 2 (a) is a case where RF signal amplitude is a large level comparatively, and it is that reference voltage V_{ref} is made into a large value, and a dynamic range can extend when such, Let A/D converter 14 be a suitable dynamic range which is provided with a moderate saturation margin to an input signal and with which a quantization error will also become small. When RF signal amplitude becomes small like drawing 2 (b), it is that reference voltage V_{ref} is made into a small value, and a dynamic range is made small, and A/D converter 14 is provided with a moderate saturation margin to an input signal, and let it be a suitable dynamic range also with a small quantization error.

[0036] Although the dynamic range control circuit 19 performs such dynamic range variable control fundamentally, especially as an example of a 1st embodiment, optimal dynamic range variable control is performed according to the various signals from the control signal generating section 21.

[0037] The various signals generated from the control signal generating section 21 are as follows. The timing reference signal TR is a signal used as the standard of the detection timing of sample data SD, for example, it is preferred for it to use the switching pulse (SWP) in sync with the head switching of the playback head 9 of the couple which serves as a reverse azimuth mutually, etc. as the timing reference signal TR.

[0038] The stationary state desired value M1 is a desired value for setting up a dynamic range comparatively small as a standard dynamic range. The special state target values M2 are desired values for setting up the comparatively large dynamic range as a standard dynamic range.

[0039] Special state detection signal SS is taken as the signal set to "H" from the search operation and operational mode transition time in a prescribed period. That is, the period which is performing the rapid-traverse search or the rewinding search about playback of the magnetic tape 90 is set to "H." With the time of operational mode transition, a reproduction → stop, reproduction → record, a reproduction → rapid-traverse search, Reproduction → A rewinding search, a stop → rapid-traverse search, a stop → rewinding search, Record → reproduction, a record → rapid-traverse search, record → it rewinds, and after a search etc. say the thing at the time of all change of operational mode and such operational mode change generates them, as for a prescribed period, special state detection signal SS is set to "H." That it is in change and the search state of operational mode detects the control signal generating section 21 with the signal from the system controller (microcomputer) which is not illustrated, for example, and a circuit system which sets special state detection signal SS to "H" by it should just be formed. Or naturally it is also possible to operate the system controller itself as the control signal generating section 21.

[0040] It detects that reproduction motion rushed into the existing recording part from the non-recording part on the magnetic tape 90, or that reproduction motion rushed into the non-recording part from the existing recording part on the magnetic tape 90 from an RF signal state, and may be made to set special state detection signal SS to "H" also in that case.

[0041] By the way, as a dashed line shows drawing 1, the output of the digital equalizing circuit 15 is also supplied to the dynamic range control circuit 19, but this serves as composition in case a 4th and 5th embodiment mentioned later is adopted.

[0042] Drawing 3 shows the important section of the example of the book as a 1st embodiment. The dynamic range control circuit 19 comprises the rectification circuit 31, the peak detection circuit 32, the timing generation part 33, the subtractor 34, the low pass filter 35, the multiplier 36, and the switch 37.

[0043] Sample data SD from A/D converter 14 is rectified in the rectification circuit 31. The situation of the rectifying operation of drawing 4 (a) and (b) is shown. When A/D converter 14 is an 8-bit A/D converter, for example, sample data SD can take the value from a positive value to a negative value like drawing 4 (a), it serves as 8 bit data. That is, as a quantized value of sample data SD, it is distributed to -128~+127. It is rectified in the rectification circuit 31 (absolute-value-izing), and this sample data SD serves as data of only a positive value like drawing 4 (b).

[0044] Rectified sample data SDS is supplied to the peak detection circuit 32. The peak detection circuit 32 comprises the 51 or 8 bits of comparator flip-flop 52, and the switch 53 like drawing 5. A clear signal is supplied to the 8-bit flip-flop 52 from the timing generation part 33. Clock CK from PLL circuit 13 is supplied as a latch clock. Rectified sample data SDS is supplied to the comparator 51 and Ti terminal of the switch 53.

[0045] The comparator 51 compares size about the latch output of sample data SDS and the flip-flop 52 which are inputted, and controls the switch 53 by the comparison result. That is, only when sample data SDS is larger, the switch 53 is connected to Ti terminal, and sample data SDS is stored up in the flip-flop 52. The value which connects the switch 53 to To terminal when the latch output of the flip-flop 52 is larger than sample data SDS, therefore is accumulated in the flip-flop 52 is maintained as it is. The latch output of the flip-flop 52 serves as peak detection value PK.

[0046] This peak detection operation becomes like drawing 4 (c) - (e). The timing generation part 33 generates the clear signal CLR like drawing 4 (d) to the flip-flop 52 according to the timing reference signal TR like drawing 4 (c). The flip-flop 52 is cleared by this clear signal CLR, and the latch output of the flip-flop 52 is measured from sample data SDS from that time. Since the accumulation value of the flip-flop 52 is updated if sample data SDS is larger, peak detection value PK becomes like drawing 4 (e). When the clear signal CLR is generated by one track of the reproduction motion on the magnetic tape 90 to 1 time of timing, peak detection value PK is obtained by 1 track unit.

[0047] Peak detection value PK is supplied to the subtractor 34, and the desired value M is subtracted. And the error E, i.e., the difference of a peak value and the desired value M, acquired by the subtraction is supplied to the low pass filter 35. As the low pass filter 35 is shown in

drawing 4 (f) from the timing generation part 33, clock (LPF clock) CK_L is supplied rather than the clear signal to the timing which carried out prescribed period delay, and smooth operation is performed based on this LPF clock CK_L . That is, the error E in the timing from which peak detection value PK of the flip-flop 52 became a peak value in 1 track correctly serves as a candidate for data smoothing. And in the low pass filter 35, smoothing is performed for the error E inputted between the errors E about a part for a neighboring track, i.e., the number track of the past, the multiplication of the coefficient alpha will be carried out with the multiplier 36, and the smoothed signal EAV will be outputted to D/A converter 20.

[0048]As a result of such a series of operations, when peak detection value PK is smaller than the desired value M, the output value to D/A converter 20 becomes small, and thereby, the dynamic range of A/D converter 14 is corrected in the direction which becomes small.

Conversely, if peak detection value PK is larger than the desired value M, the dynamic range of A/D converter 14 will be corrected in the direction which becomes large.

[0049]When sample data SD shall take the value of $-128 \sim +127$ here, I think that M was set as the desired value +110. Then, it will be controlled for the peak value of sample data SD of a one track period to average in this case, and to be set to ± 110 . In this case, the surplus ratio to the saturation in A/D converter 14 is $\{(127-110)/110\} \times 100 = 15\%$.

It comes out.

[0050]What is necessary is on the other hand, just to make the desired value M small for the increase in a quantization error, when [a certain] thinking that he would like to increase a saturation surplus ratio, even if it carries out grade permission. For example, it is set as the desired value $M+50$. Since the dynamic range of A/D converter 14 at this time will change in the direction which becomes large to the input signal amplitude to A/D converter 14, a saturation surplus ratio increases. Namely, $\{(127-50)/50\} \times 100 = 154\%$

It becomes. That is, it will not be saturated until the input to A/D converter 14 large-amplitude-izes 2.54 times suddenly.

[0051]When there is a possibility that large amplitude-ization [**** / as an input from the above thing to A/D converter 14] may occur, it is understood that what is necessary is to make the value of the desired value M small and just to make a saturation margin high. So, in this example, the control signal generating section 21 supplies two values, the stationary state desired value M1 and the special state target values M2, to 37Tswitch 1 terminal and T2 terminal as a value which can be used as the desired value M, respectively. The stationary state desired value M1 sets up a comparatively small dynamic range, and is made into the value for lessening a quantization error, for example, is made into $M1 = "110"$. The special state target values M2 are desired values for setting up a dynamic range comparatively large even if it carries out grade permission, in order [a certain] to enlarge a saturation margin, for example, the increase in a quantization error is made into $M2 = "50"$.

[0052]And the control signal generating section 21 supplies special state detection signal SS set to "H" from the search operation and operational mode transition time in a prescribed period to the dynamic range control circuit 19 as a switching control signal of the switch 37, as mentioned above. If special state detection signal SS is set to "H", T2 terminal will be connected to the switch 37, and as for the switch 37, T1 terminal will be connected if special state detection signal SS is set to "L."

[0053]It is the period when special state detection signal SS is "L" at the usual reproduction motion time (stationary state), and the stationary state desired value M1 is supplied to the subtractor 34 as the desired value M at this time. Therefore, when $M1 = "110"$, as mentioned above, a saturation surplus ratio is 15% and the dynamic range of A/D converter 14 will be controlled to an input signal by the suitable state with few quantization errors. On the other hand, in a prescribed period, a (special state) and the special state target values M2 are supplied to the subtractor 34 as the desired value M from the period, at i.e., the search operation and operational mode transition time, when special state detection signal SS is "H." Therefore, if $M1 = "50"$, as mentioned above, a saturation surplus ratio is 154%, and as for the dynamic range of A/D converter 14, although a quantization error is large, it will be controlled to an input signal

by the state where it had sufficient saturation margin.

[0054]The situation of dynamic range control is typically shown in drawing 6. Suppose that operational mode changed to the time base direction (at the $t_1 - t_6$ time) with the stop \rightarrow reproduction \rightarrow rapid-traverse (FF) search \rightarrow rewind (REW) search \rightarrow reproduction \rightarrow stop. Drawing 6 (a) shows change of the desired value M, and drawing 6 (b) shows change of a saturation surplus ratio.

[0055]After reproduction is first started from a halt condition, since special state detection signal SS is set to "H", the special state target values M2 are used as the desired value M, fixed time's ($t_0 - t_1$) dynamic range is large, that is, a large saturation margin is taken at it. If it goes through predetermined time and special state detection signal SS is set to "L" ($t_1 - t_3$), the stationary state desired value M1 is used as the desired value M, and although a dynamic range is small and a saturation margin is small, it will change a quantization error into a small state.

[0056]If it shifts to a rapid-traverse search from t_2 time, special state detection signal SS will be set to "H", a dynamic range will be enlarged, and, as for the rewind search at the $t_3 - t_4$ time, this state will be continued. Even if it furthermore shifts to reproduction motion at the t_4 time, till t_5 point in time which is a prescribed period from mode change, special state detection signal SS is still "H", and the state where the dynamic range was enlarged is continued. and t_5 time or subsequent ones -- t_6 time -- until -- it changes a dynamic range into the small state where a quantization error is small, as a stationary state.

[0057]Namely, in this example, an input signal makes the dynamic range of A/D converter 14 small according to a certain stationary state which is carrying out grade stability, Aim at improvement in an error rate by lessening a quantization error, and on the other hand, when there is a possibility of causing change with a sudden input signal to A/D converter 14, the time of a search and mode change, etc., Even if a certain grade permits a quantization error, the dynamic range of A/D converter 14 is enlarged and an error is prevented from increasing to a degree very much by taking sufficient saturation margin so that the situation of overflow which must be avoided most may not occur.

[0058][A 2nd embodiment] Drawing 7 and drawing 8 explain the example as a 2nd embodiment. The composition as [whole] a recording and reproducing device presupposes that it is the same as that of drawing 1, and only an important section is shown in drawing 7.

[0059]A different point from the dynamic range control circuit 19 in a 1st embodiment of the above in the dynamic range control circuit 19 in this example, It is the point of performing operation by which there is no switch 37, the fixed desired value's M being supplied to the subtractor 34 from the control signal generating section 21 and special state detection signal SS are inputted into the low pass filter 35, and special state detection signal SS controls the response time constant of the low pass filter 35.

[0060]Although the low pass filter 35 is formed as for example, an IIR digital filter, the common model of an IIR digital filter is shown in drawing 8 (a). That is, the multiplication of the input data is carried out to the coefficient K with the multiplier 71, and via the adding machine 72, it is delayed 1 sample timing and outputted in the delay circuit 73. The multiplication of the output of the delay circuit 73 is carried out to a coefficient $(1-K)$ with the multiplier 74 again, and it is fed back to the adding machine 72. It is known for such an IIR digital filter that a response time constant will change with the values of the coefficient K (and $1-K$).

[0061]So, in this example, the speed of response of a dynamic range control loop is changed by making it change the value of the coefficient K (and $1-K$) based on special state detection signal SS.

[0062]The period when special state detection signal SS is "L" is at the usual reproduction motion time (stationary state), as mentioned above, and an amplitude change rapid as an input of A/D converter 14 at this time does not appear. and -- in order to raise the stability of a dynamic range control loop -- the response as the dynamic range control circuit 19 -- a certain grade -- it is better to make it late. Then, the low pass filter 35 sets the period when special state detection signal SS is "L", for example to coefficient $K = 0.1$ and coefficient $(1-K) = 0.9$. then, the response time constant of the low pass filter 35 -- drawing 8 (b) -- like -- a certain grade -- it changes into a late state.

[0063]On the other hand, in a prescribed period, a (special state) and an amplitude change rapid as an input of A/D converter 14 may arise from the period, at i.e., the search operation and operational mode transition time, when special state detection signal SS is "H." In such a case, it is necessary to react immediately as dynamic range control operation, and to avoid overflow and increase of a quantization error. Then, the low pass filter 35 sets the period when special state detection signal SS is "H", for example to coefficient $K=0.3$ and coefficient $(1-K)=0.7$, and changes a response time constant into a quick state like drawing 8 (c).

[0064]In such this example, answer immediately [when an amplitude change rapid as an input of A/D converter 14 arises in the time of a search, etc.], and the dynamic range of A/D converter 14 is changed properly, Overflow and increase of a quantization error can be avoided and, on the other hand, always [constant], a late response can realize stability of a dynamic range control loop moderately.

[0065][A 3rd embodiment] Drawing 9 explains the example as a 3rd embodiment. The composition as [whole] a recording and reproducing device presupposes that it is the same as that of drawing 1, and only an important section is shown in drawing 9. A different point from the example as a 2nd embodiment which this example mentioned above is a point of having formed the positive/negative evaluating part 38. About the value of the error E which is an output of the subtractor 34, the positive/negative evaluating part 38 distinguishes a positive value or a negative value, and supplies it to the low pass filter 35 by making the discriminated result into the time number change signal J.

[0066]As operation of the dynamic range control 19, When the error E is a negative value when peak detection value PK is smaller than the desired value M namely, as mentioned above, It controls so that the dynamic range of A/D converter 14 becomes small, and on the other hand, when the error E is a positive value when peak detection value PK is larger than the desired value M namely, it controls so that the dynamic range of A/D converter 14 becomes large. The positive/negative evaluating part 38 distinguishes whether the present processing controls by positive/negative judgment of the error E to become small about whether it controls so that a dynamic range becomes large. And the damping time constant of the low pass filter 35 will be controlled by the discriminated result.

[0067]drawing 8 (b) which the low pass filter 35 set, for example to coefficient $K=0.1$ and coefficient $(1-K)=0.9$, and was mentioned above when it was distinguished that the error E is negative -- like -- the response time constant of the low pass filter 35 -- a certain grade -- it changes into a late state. On the other hand, when it is distinguished that the error E is positive, it is made for the low pass filter 35 to set to coefficient $K=0.3$ and coefficient $(1-K)=0.7$, and it changes a response time constant into a quick state like drawing 8 (c).

[0068]That is, in the dynamic range control circuit 19 of this example, when expanding the dynamic range of A/D converter 14, a response is made quick. The time of expanding a dynamic range is a time of the input signal amplitude to A/D converter 14 becoming large, that is, is a time of a possibility that overflow will arise occurring. Therefore, when such, it is performing expansion control of a dynamic range by a quick response, and overflow generating is prevented. That is, it can be said that it is what strengthens the preventing function to the overflow which must not take place most.

[0069][A 4th embodiment] The important section of a 4th embodiment is shown in drawing 10. It is the point which he is trying to supervise also about the output of the digital equalizing circuit 15 as a feature of the dynamic range control circuit 19 in this example as the dashed line showed also to drawing 1. In this example, sample data SD which is an output of A/D converter 14 is inputted into the rectification circuit 31A, and is set to sample data SDS1 rectified. The output of the digital equalizing circuit 15 is inputted into the rectification circuit 31B, and is set to data SDS2 rectified similarly.

[0070]Sample data SDS1 rectified in the rectification circuit 31A is supplied to TS1 terminal and the comparator 39 of the switch 40. Data SDS2 rectified in the rectification circuit 31B is supplied to TS2 terminal and the comparator 39 of the switch 40.

[0071]The comparator 39 performs size comparison about the value of data SDS1 inputted and SDS2, and outputs the comparison result as a control signal over the switch 40. That is, if data

SDS1 is larger, terminal TS1 will be connected to the switch 40, and if data SDS2 is larger, terminal TS2 will be connected to the switch 40.

[0072]Therefore, the data of the larger one as an absolute value among the outputs of sample data SD outputted from A/D converter 14 and the digital equalizing circuit 15 will be supplied to the peak detection circuit 32, and will be made into the object of peak detection operation. And like each example mentioned above, peak detection value PK and the desired value M are subtracted with the subtractor 34, and variable control of a dynamic range is performed according to the acquired error E.

[0073]In such this example, the digital equalizing circuit 15 will also be included in a dynamic range control loop. Even if overflow does not occur in A/D converter 14, there will also be a possibility that sample data may overflow by the operation in the digital equalizing circuit 15. What is necessary is just to enlarge the dynamic range of A/D converter 14, when there is such fear in order to prevent the overflow in the digital equalizing circuit 15.

[0074]By then, the thing for which the digital equalizing circuit 15 is also included in a dynamic range control loop like this example, both the output of the digital equalizing circuit 15 and the output of A/D converter 14 are supervised, and peak detection is performed. The dynamic range control of A/D converter 14 kept from generating the overflow in the digital equalizing circuit 15 is attained.

[0075][A 5th embodiment] The important section of a 4th embodiment is shown in drawing 11. This example is provided with all the features of the 1st explained so far – the dynamic range control circuit as a 4th embodiment.

[0076]That is, like a 1st embodiment, it is made for the switch 37 to switch according to special state detection signal SS, that is, the desired value M is switched to the stationary state desired value M1 and the special state target values M2 by special state detection signal SS. Thereby, in a regular reproduction state, few, at the time of a search, a dynamic range is enlarged at the time of mode transition, and a saturation margin is acquired [with a small dynamic range] also to a sudden large amplitude input the time in a quantization error.

[0077]Like a 2nd embodiment, while changing the response time constant of the low pass filter 35 by special state detection signal SS, even if it responds to positive/negative evaluation of the error E like a 3rd embodiment, the response time constant of the low pass filter 35 is changed. For this reason, special state detection signal SS is supplied to the low pass filter 35 via OR gate 41, and the damping time constant change signal J from the positive/negative evaluating part 38 is supplied to the low pass filter 35 via OR gate 41.

[0078]Therefore, at the time of a search, at the time of mode transition, it changes the low pass filter 35 into a high speed response state, and also when it carries out expansion control of the dynamic range further, it changes it into a high speed response state. Even if an amplitude change rapid as an input of A/D converter 14 arises by this, answer immediately and the dynamic range of A/D converter 14 is changed properly, A response is made quick so that overflow and increase of a quantization error can be avoided, and on the other hand, always [constant], the stability of a dynamic range control loop is moderately obtained as a late response. It enables it to avoid overflow certainly by changing into a high speed response state also at the time of the dynamic range expansion with fear of overflow.

[0079]Since he is trying to incorporate the output of the digital equalizing circuit 15 as well as [still] a 4th embodiment into a dynamic range control loop, not only A/D converter 14 but the function of the prevention from overflow in the digital equalizing circuit 15 will be exhibited.

[0080]

[Translation done.]

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【特許請求の範囲】

【請求項1】 記録媒体から読み出されたRF信号をA/D変換手段でデジタルデータに変換してデコード処理を行ないデータを再生するデータ再生装置において、前記A/D変換手段におけるダイナミックレンジを可変制御できるダイナミックレンジ制御手段を備え、

このダイナミックレンジ制御手段は、当該データ再生装置の動作が定常状態であるときはダイナミックレンジを小さく、また当該データ再生装置の動作が特殊状態であるときはダイナミックレンジを大きくするように制御を行なうことを特徴とするデータ再生装置。

【請求項2】 前記特殊状態であるときは、当該データ再生装置がサーチ動作を行なっている期間及び/又は動作モードが遷移したときの所定期間とすることを特徴とする請求項1に記載のデータ再生装置。

【請求項3】 記録媒体から読み出されたRF信号をA/D変換手段でデジタルデータに変換してデコード処理を行ないデータを再生するデータ再生装置において、前記A/D変換手段におけるダイナミックレンジを前記A/D変換手段の出力に応じて適応的に可変制御できるダイナミックレンジ制御手段を備え、

このダイナミックレンジ制御手段は、当該データ再生装置の動作が定常状態であるときは前記A/D変換手段の出力に応じたダイナミックレンジ可変制御動作の応答性が遅くなるように設定され、また当該データ再生装置の動作が特殊状態であるときは前記A/D変換手段の出力に応じたダイナミックレンジ可変制御動作の応答性が早くなるように設定されることを特徴とするデータ再生装置。

【請求項4】 前記特殊状態であるときは、当該データ再生装置がサーチ動作を行なっている期間及び/又は動作モードが遷移したときの所定期間とすることを特徴とする請求項3に記載のデータ再生装置。

【請求項5】 記録媒体から読み出されたRF信号をA/D変換手段でデジタルデータに変換してデコード処理を行ないデータを再生するデータ再生装置において、前記A/D変換手段におけるダイナミックレンジを前記A/D変換手段の出力に応じて適応的に可変制御できるダイナミックレンジ制御手段を備え、

このダイナミックレンジ制御手段は、前記A/D変換手段のダイナミックレンジを拡大する制御を行なう際には、前記A/D変換手段の出力に応じたダイナミックレンジ可変制御動作の応答性が早くなるように設定されることを特徴とするデータ再生装置。

【請求項6】 記録媒体から読み出されたRF信号をA/D変換手段でデジタルデータに変換し、等化手段で等化処理を行なってからデコード処理を行ないデータを再生するデータ再生装置において、前記A/D変換手段の出力及び前記等化手段の出力の両方を監視して、前記A/D変換手段におけるダイナミッ

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ックレンジを適応的に可変制御できるダイナミックレンジ制御手段を備えたことを特徴とするデータ再生装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、記録媒体から読み出された信号をデジタルデータに変換して等化処理やデコード処理を行ない、データを再生するデータ再生装置に関するものである。

【0002】

【従来の技術】磁気テープ、磁気ディスク、光ディスク、光磁気ディスクなど、各種の記録媒体及びそれに対応する記録再生装置が普及している。近年の高密度デジタル記録システムにおける再生装置では、再生ヘッドによって記録媒体から読み出された信号(RF信号)に対してアナログイコライザやデジタルフィルタによる等化処理を行ない、等化されたRF信号をA/D変換する。そしてデジタルデータに対して等化処理、2値化処理、デコード処理、エラー訂正処理等を行なってデータを再生することが多い。これは、高密度デジタル記録システムのRF信号処理技術として、等化方式をパーシャルレスポンス方式、検出方式を最尤検出法(ビタビ検出:ビタビ検出:Maximum Likelihood Detection Method)という組み合わせ(PRML方式)を採用する例が増えているためである。

【0003】例えばDAT(デジタルオーディオテープ)記録再生装置を例にあげると、従前は積分等化を採用し、RF処理としてはアナログリミッタで2値化を行ない、デコード及びエラー訂正という簡単な構成で済んでいたが、PRML方式を採用した場合は、ビタビ検出動作が、等化されたRF信号の検出点電圧系列(サンプリングデータ系列)をデジタル信号処理することで2値化する仕組みであるため、RF信号をサンプリングするためのA/D変換器が必要となる。

【0004】ところが、A/D変換器はアナログーデジタル変換可能な信号入力範囲として固有のダイナミックレンジを持ち、ダイナミックレンジに比べて入力信号レベルが適正範囲でない場合は良好なサンプルデータが得られず、検出エラーが多発するという事態が生ずる。

【0005】即ちダイナミックレンジに比べて著しく小さい振幅のRF信号が入力された場合は、A/D変換器の出力(サンプルデータ)中の量子化誤差が増大し、SN比が悪化するため検出エラーが増加する。またダイナミックレンジを越えるような大振幅のRF信号が入力された場合は、サンプルデータは飽和したデータとなり、即ちA/D変換動作における直線性が損なわれてしまう。このようなサンプルデータのSN比は極度に劣化しており、検出エラーは大幅に増加する。

【0006】これらの状況を図12～図25で説明する。RF信号をクラス1パーシャルレスポンス方式(P R(1,1)方式)で等化された波形であるとして説明す

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る。図12はクラス1バーチャルレスポンス等化波形のアイパターンである。この等化波形は、図中○で示すサンプルポイント（検出点）で「1」「0」「-1」の3種類の値を取りうる。しかし現実の波形はノイズを含むのでこの図のようにサンプルポイントで1点に収束することとはなくばらつく。

【0007】このような波形をサンプリングすると、図13のような、3つの電圧を中心に分布したサンプルデータ分布が得られる。この図13はRF信号をA/D変換器でサンプリングしたサンプルデータ値（電圧値）を30000ポイント表示したグラフである。これはA/D変換器の精度を8ビット（-128～+127）とし、A/D変換器のダイナミックレンジを概略図14のように設定したときの状態である。つまり図14のようにRF信号波形の振幅（斜傾部）に対してA/D変換器のダイナミックレンジとして或る程度の飽和余裕をとり、RF信号振幅に対してA/D変換器のダイナミックレンジがだいたい適正な状態に設定されているとされる場合である。このような場合は、図13のように、ほぼ±1000ポイントのサンプリングデータ分布が得られ

た。【0008】次に、RF信号電圧（振幅）が図15のように、図14に比べてほぼ半分になった場合について考えてみる。このときのサンプルデータ分布は図16のようになる。図16のグラフは前記図13と同スケールにより示したものであり、これを拡大したのが図17である。図16からわかるように、サンプルデータ分布は約±500ポイントの範囲の分布となり、特に図13に対して図17を比較してわかるようにサンプルデータ分布はまばらになっている。これはA/D変換器のダイナミックレンジに対してRF信号振幅が小さくなることで量子化誤差が増加していることを意味する。

【0009】さらに、RF信号電圧（振幅）が図14の状態に比べて約1/4、約1/8となった場合の分布をそれぞれ図18、図20に示す。図18、図20は前記図13と同スケールにより示したものであり、図18を拡大したのが図19、図20を拡大したのが図21である。これらの図からは、サンプルデータ分布はさらにまばらになっていることが観測され、つまりA/D変換器のダイナミックレンジに対してRF信号振幅が小さくなっていくほど量子化誤差が増加していくことが理解される。

【0010】次に、RF信号振幅がA/D変換器のダイナミックレンジを超えるようなものとなった場合を考える。図22は、図23に示すようにA/D変換器のダイナミックレンジを設定した場合のサンプルデータの分布を示している。つまり、図14のようにダイナミックレンジが標準的なものとなっている場合に比べてRF信号振幅が約1.5倍となった例である。図22の分布状態では、サンプルデータの値の最大値は+127、最小値は

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-128に制限され、飽和していることが観測される。RF信号電圧が約1.5倍大きくなるような変化をしたに過ぎないが、これによってA/D変換動作の直線性が損なわれる。そしてこのようなサンプルデータ系列に対してはビタビ復号は正常動作せず、エラーが多発することになる。

【0011】さらに図24は、図25に示すようにA/D変換器のダイナミックレンジを設定した場合のサンプルデータの分布を示している。これは図14のようにダイナミックレンジが標準的なものとなっている場合に比べてRF信号振幅が約2倍となった例である。この図24の分布状態でもサンプルデータの値の最大値は+127、最小値は-128に制限され、飽和していることが観測される。そしてRF信号電圧が約2倍大きくなることによりA/D変換動作の直線性は大きく損なわれ、このようなサンプルデータ系列に対してはビタビ復号は正常動作せず、エラーはより多発することになる。

【0012】以上のようにダイナミックレンジに比べて入力信号レベルが適正範囲でない場合はA/D変換器から良好なサンプルデータが得られず、検出エラーが多発することになる。このような事情に対して本出願人は先行技術として特開平6-183945号に記載した提案を行なった。この特開平6-183945号には、A/D変換器の出力に応じてA/D変換器の入力レベルを制御するAGC回路（オートゲインコントロール回路）を設けることで、入力信号をA/D変換器のダイナミックレンジに対して適切なレベルとする技術が記載されている。

【0013】【発明が解決しようとする課題】A/D変換器の入力信号に対するAGC回路を設けることで、通常は、A/D変換器のダイナミックレンジに対する入力信号レベルを適正範囲とさせることができるが、以下のような問題点が残されている。

【0014】再生装置では、再生動作、サーチ動作など、動作モードが遷移するとき、再生動作が記録媒体上の未記録部分から既記録部分に突入したとき、再生動作が記録媒体上の既記録部分から未記録部分に突入したとき、などはRF信号レベルが大きく変動することがある。

【0015】上述したA/D変換器のダイナミックレンジと入力信号レベルの関係としてはこのような場合に生ずる突発的な振幅増大にも対処可能とすることが必要であるが、このためには予めダイナミックレンジを大きめに設定しておくことが必要である。即ち飽和余裕を持たせることである。ところが、このような場合は量子化誤差が増大することにもなる。つまりAGC回路による通常時の入力レベル制御だけでは従って量子化誤差の減少と突発的大振幅への対応という2つの要件を満たすことができない。

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【0016】また、入力信号振幅の突発的变化についてAGC回路の応答性を考えると次のような問題が生ずる。まずRF信号振幅が小レベルから大レベルに突発的に変化する時は、それまでA/D変換器のダイナミックレンジに対しては小レベル信号が適正状態となるようにAGC制御されているため、突然の大振幅入力時には相対的にダイナミックレンジが過小なものとなってしまう。よってAGC回路が大振幅入力に対応してゲインを適正状態に下げるまでの期間は、サンプルデータは飽和するため、SN比は大きく劣化しエラーが極度に増加する。従って、このような場合に大振幅に即座に反応できるようにAGC回路には迅速な応答性が求められる。

【0017】またRF信号振幅が大レベルから小レベルに突発的に変化する時は、ダイナミックレンジがそれまでの大振幅RF信号に適応している状態であるので、小レベル入力に対して相対的にダイナミックレンジが過大なものになってしまう。このため量子化誤差が増大し、この場合もSN比の劣化、エラーの増大が生ずる。従って、この場合にもAGC回路には迅速な応答性が求められる。

【0018】ところが応答速度を速めると、収束性が悪くAGCループが不安定になる。このため、突発的な振幅変化に十分対応できるほど高速応答化を行なうことはできなかった。そして高速応答化の困難な事情から、コンピュータデータストレージ機器などのように頻りに再生/サーチなどの動作モードが変化する機器では、特に不利なものとなっていた。つまり、AGC回路が安定するまでのオーバーヘッドが長くなり、これによって機器の反応速度が遅くなるためである。

【0019】さらにデジタル等化回路を備えた装置について考えると、A/D変換器の出力段階でサンプルデータが飽和していても、デジタル等化回路の演算によりデータにオーバーフローが生ずる恐れがある。特に等化特性を自動調整（適応等化）する機器の場合は、等化特性の変化を予測できないため、等化回路の出力信号についても監視を行なうことが求められている。

【0020】

【課題を解決するための手段】本発明は以上のような問題点に鑑みてA/D変換手段のダイナミックレンジと入力信号レベルが常に適切な状態となるように制御可能とするとともに、A/D変換手段のダイナミックレンジを大きくして飽和余裕を得ることと量子化誤差を小さくするという相反した要件を場合分けにより満足できるようにすること、制御ループの安定性と応答速度の高速化という相反する要件を場合分けにより満足できるようにすること、必要なときには量子化誤差対策よりも飽和対策を優先すること、デジタル等化を行なう場合には、そのデジタル等化処理における飽和防止も実現すること、を目的とする。

【0021】このため、まずA/D変換手段におけるダ

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イナミックレンジを可変制御できるダイナミックレンジ制御手段を備え、このダイナミックレンジ制御手段は、当該データ再生装置の動作が定常状態であるときはダイナミックレンジを小さく、また当該データ再生装置の動作が特殊状態であるときはダイナミックレンジを大きくするように制御を行なう。つまりA/D変換手段のダイナミックレンジと入力信号レベルが常に適切な状態となるようにダイナミックレンジを可変制御するとともに、突発的な振幅変化が殆ど発生しないと思われる定常状態では、A/D変換手段のダイナミックレンジを小さくして量子化誤差を小さくするが、突発的な振幅変化が発生する恐れのある特殊状態ではダイナミックレンジを大きくして飽和余裕を大きくし、オーバーフローを防止する。

【0022】また、A/D変換手段におけるダイナミックレンジをA/D変換手段の出力に応じて適応的に可変制御できるダイナミックレンジ制御手段を備え、このダイナミックレンジ制御手段は、当該データ再生装置の動作が定常状態であるときはA/D変換手段の出力に応じたダイナミックレンジ可変制御動作の応答性が遅くなるように設定され、また当該データ再生装置の動作が特殊状態であるときはA/D変換手段の出力に応じたダイナミックレンジ可変制御動作の応答性が早くなるように設定されるようにする。つまりA/D変換手段のダイナミックレンジと入力信号レベルが常に適切な状態となるようにダイナミックレンジを可変制御するとともに、突発的な振幅変化が殆ど発生しないと思われる定常状態では、制御の応答性を遅くして安定性を優先させ、突発的な振幅変化が発生する恐れのある特殊状態では応答性を速くして振幅変化に即座に対応できるようにする。

【0023】また、A/D変換手段におけるダイナミックレンジをA/D変換手段の出力に応じて適応的に可変制御できるダイナミックレンジ制御手段として、A/D変換手段のダイナミックレンジを拡大する制御を行なう際には、A/D変換手段の出力に応じたダイナミックレンジ可変制御動作の応答性が早くなるようする。つまり、ダイナミックレンジ拡大時にはオーバーフロー対策を最優先させる。

【0024】また、A/D変換手段の出力及び前記等化手段の出力の両方を監視して、A/D変換手段におけるダイナミックレンジを適応的に可変制御できるダイナミックレンジ制御手段を設けることで、A/D変換処理とデジタル等化処理の両方に関して飽和防止を実現する。

【0025】

【発明の実施の形態】以下、本発明の各種実施の形態としてのデータ再生装置を、DAT記録再生装置として実現する例で説明する。なお、この例は音声データをデジタル化して記録/再生するDAT記録再生装置とするが、コンピュータデータ等を対象としたデータストレージ機器としてDATシステムやその他の磁気テープメ

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ィアが用いられるシステム、磁気ディスクシステム、光磁気ディスクシステム、光ディスクシステムであっても、本発明は同様に適用できるものである。

【0026】〔第1の記録の形態〕図1は磁気テープに対しての音声信号の記録／再生を行なうD/A記録再生装置のブロック図である。記録されるアナログ音声信号は端子1から入力されてA/D変換器2でデジタルデータに変換される。そして、エラー訂正用エンコード部3で所定のデータ単位毎にエラー訂正コードが付加され、記録用のフォーマットとしてのデジタルデータが生成される。このデジタルデータは8-10変調部4で8-10変調処理されて記録用の信号とされ、プリコーダ5を介して記録アンプ6に供給される。この記録用の信号としては、次のロータリトランス7を介し、ここで直流(DC)成分がカットされることから、DCフリーの符号別である8-10変調が採用されているものである。またプリコーダ5は例えばクラス1パーシャルレスポンス(PR(1,1))におけるプリコーダである。

【0027】記録アンプ6で増幅された信号はロータリトランス7を介して回転ドラム内の記録ヘッド8に供給され、記録ヘッド8により走行されている磁気テープ9に対して磁気記録動作が行なわれる。図示しないが記録ヘッド8を搭載した回転ドラムに対しては磁気テープ9は高さ方向に傾斜した状態で所要角度巻きつけられながら走行し、また回転ドラムは磁気テープ9に接触しながら回転されることで、いわゆるヘリカルスキャン方式による記録トラックが形成されていく。

【0028】再生時には、回転ドラムに巻きつけられた磁気テープ9が走行されるとともに回転ドラムが回転されることで、回転ドラムに搭載されている再生ヘッド9が記録トラックをトレースしていき、記録されたデータが読み出される。なお、図面上は1つの記録ヘッド8、1つの再生ヘッド9を示しているのみであるが、実際にはアジマスベタ記録方式が採用されるため、アジマス角度の異なる2つの記録ヘッド、2つの再生ヘッドがそれぞれ互いに所定角度離れた状態で回転ドラムの周面上に配置されていることになる。実際の形態としては2つの記録専用ヘッドと2つの再生専用ヘッドが用いられる場合、2つの記録再生ヘッドが用いられる場合、1つの記録再生ヘッドと各1つの記録ヘッド、再生ヘッドが採用される場合等がある。

【0029】再生ヘッド9で読み出された信号はロータリトランス10を介して再生アンプ11に供給される。なお、実際には記録用のロータリトランス7と再生用のロータリトランス10は1つのロータリトランスで兼用できる場合もある。再生アンプ11で増幅された信号はアナログ等化回路12で等化処理されてPLL回路13及びA/D変換器14に供給される。アナログ等化回路12は、いわゆる一般的なアナログイコライザとして構成され、再生ヘッド9が有する微分特性を補

正するための低域に対して積分特性を有する積分回路と、再生ヘッド9のギャップ等によるロスを補正するための高域に対して微分特性を持つ微分回路と、必要な帯域の信号だけを通過させるローパスフィルタと、このローパスフィルタによる位相回りを補正するため振幅を変化させずに位相を変化させる位相等化器とを備える。

【0030】PLL回路13はアナログ等化回路12からの出力に同期した再生クロックCKを生成し、A/D変換器14、デジタル等化回路15、2値化回路16、10-8変換部17、エラー訂正部18に対しての動作クロックとして供給する。

【0031】アナログ等化回路12からの出力はA/D変換器14でデジタルデータ化された後、その信号(サンプルデータSD)はデジタル等化回路15に入力される。このデジタル等化回路15はトランスバースフィルタと適応等化係数計算回路から形成される。そして適応等化係数計算回路がトランスバースフィルタの出力から予測される予測誤差に応じて適応的にタップ係数を可変発生させ、トランスバースフィルタのフィルタリング処理を制御する。トランスバースフィルタではアナログ等化回路12の出力段階の信号において残留する等化誤差を最小化する働きを行なうことになるが、そのための等化特性が、適応等化係数計算回路から与えられるタップ係数により適応的に最適状態に設定されることになる。

【0032】デジタル等化回路15においてフィルタリング処理された信号は2値化回路16に供給される。2値化回路16では入力される信号を2値化し、10-8変換部17に出力する。本例の場合、PRML方式が採用されており、プリコーダ5からデジタル等化回路15の出力までの伝達特性はパーシャルレスポンス特性とされ、2値化回路16はビタビ復号を行なうものとされる。

【0033】10-8変換部17は記録時の8-10変調に対するデコード動作を行なう。デコードされたデータはエラー訂正部18でエラー訂正処理がされた後、D/A変換器25でアナログ信号とされる。つまりもとのアナログ音声信号とされる。そしてアンプ26により増幅されスピーカ27から音声として出力される。

【0034】A/D変換器14の出力であるサンプルデータSDは、ダイナミックレンジコントロール回路19にも供給される。詳しくは後述するが、ダイナミックレンジコントロール回路19はサンプルデータSDと、制御信号発生部21からの各種信号に応じてA/D変換器14のダイナミックレンジを設定する値を発生させる。その値はD/A変換器20でアナログ電圧値とされるが、そのアナログ電圧値はA/D変換器14の基準電圧Vrefとなる。つまりA/D変換器14は基準電圧がダイナミックレンジコントロール回路19により可変されることで、A/D変換動作のダイナミックレンジが可

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変されることになる。そしてダイナミックレンジコントロール回路19はA/D変換器14の出力であるサンプルデータSDの値に基づいてフィードバック制御を行なうことで、図2に模式的に示すような動作が実現される。

【0035】図2(a)はRF信号振幅が比較的大レベルであった場合であり、このようなときは基準電圧Vrefが大きい値とされダイナミックレンジが広げられることで、A/D変換器14は入力信号に対して適度な飽和余裕を備え、また量子化誤差も小さいものとなる適切なダイナミックレンジとされる。また図2(b)のようにRF信号振幅が小さくなった場合は、基準電圧Vrefが小さい値とされダイナミックレンジが小さくされることで、A/D変換器14は入力信号に対して適度な飽和余裕を備え、また量子化誤差も小さい適切なダイナミックレンジとされる。

【0036】ダイナミックレンジコントロール回路19は基本的にはこのようなダイナミックレンジ可変制御を実行するが、第1の実施の形態の例としては特に制御信号発生部21からの各種信号に応じて最適なダイナミックレンジ可変制御を行なう。

【0037】制御信号発生部21から発生される各種信号は次の通りである。タイミング基準信号TRは、サンプルデータSDの検出タイミングの基準となる信号であり、例えば互いに逆アジマスとなる一対の再生ヘッド9のヘッド切り換えに同期したスイッチングパルス(SWP)などをタイミング基準信号TRとして用いることが好適である。

【0038】定常状態目標値M1は、基準的なダイナミックレンジとして比較的小さいダイナミックレンジを設定するための目標値である。特殊状態目標値M2は、基準的なダイナミックレンジとして比較的大きいダイナミックレンジを設定するための目標値である。

【0039】特殊状態検出信号SSは、サーチ動作時、及び動作モード遷移時から所定期間において「H」となる信号とする。即ち遊気テープ90の再生に関して早送りサーチまたは巻き戻しサーチを行なっている期間は「H」となる。さらに、動作モード遷移時は、再生→停止、再生→記録、再生→早送りサーチ、再生→巻き戻しサーチ、停止→早送りサーチ、停止→巻き戻しサーチ、記録→再生、記録→早送りサーチ、記録→巻き戻しサーチ……など、動作モードのあらゆる変化時のことをいい、このような動作モード変化が発生してから所定期間は特殊状態検出信号SSが「H」となる。制御信号発生部21は、動作モードの変化やサーチ状態であることは例えば図示しないシステムコントローラ(マイクロコンピュータ)からの信号により検出し、それによって特殊状態検出信号SSを「H」とするような回路系が形成されればよい。もしくは、システムコントローラそのものを制御信号発生部21として機能させることも当然可

能である。

【0040】なお、RF信号状態から再生動作が遊気テープ90上の未記録部分から既記録部分に突入したこと、又は再生動作が遊気テープ90上の既記録部分から未記録部分に突入したことを検出して、その際にも特殊状態検出信号SSを「H」とするようにしてもよい。

【0041】ところで図1においては縦線で示すようにデジタル等化回路15の出力もダイナミックレンジコントロール回路19に供給されているが、これは後述する第4、第5の実施の形態が採用される場合の構成となる。

【0042】図3は第1の実施の形態としての本例の要部を示す。ダイナミックレンジコントロール回路19は、整流回路31、ピーク検出回路32、タイミング発生部33、減算器34、ローパスフィルタ35、乗算器36、スイッチ37から構成されている。

【0043】A/D変換器14からのサンプルデータSDは整流回路31において整流される。図4(a)

(b)の整流動作の様子を示す。A/D変換器14は8ビットA/D変換器であるとした場合、サンプルデータSDは図4(a)のように正値から負値までの値をとりうる例えば8ビットデータとなる。即ちサンプルデータSDの量子化値としては-128～+127まで分布する。このサンプルデータSDは整流回路31で整流(絶対値化)され、図4(b)のように正値のみのデータとなる。

【0044】整流されたサンプルデータSDはピーク検出回路32に供給される。ピーク検出回路32は例えば図5のようにコンパレータ51、8ビットフリップフロップ52、スイッチ53から構成される。8ビットフリップフロップ52にはクリア信号がタイミング発生部33から供給される。またPLL回路13からのクロックCKがラッチクロックとして供給されている。整流されたサンプルデータSDはコンパレータ51及びスイッチ53のTi端子に供給される。

【0045】コンパレータ51は入力されるサンプルデータSDとフリップフロップ52のラッチ出力について大小の比較を行ない、その比較結果によりスイッチ53の制御を行なう。即ち、サンプルデータSDの方が大きいときのみスイッチ53をTi端子に接続し、サンプルデータSDをフリップフロップ52に蓄積させる。サンプルデータSDよりフリップフロップ52のラッチ出力の方が大きいときはスイッチ53をTo端子に接続し、従って、フリップフロップ52に蓄積される値はそのまま維持される。フリップフロップ52のラッチ出力はピーク検出値PKとなる。

【0046】このピーク検出動作は図4(c)～(e)のようになる。タイミング発生部33は図4(c)のようなタイミング基準信号TRに応じて、フリップフロップ52に対して図4(d)のようなクリア信号CLRを

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発生させる。このクリア信号CLRによりフリップフロップ52はクリアされ、その時点からサンプルデータSDSよりフリップフロップ52のラッチ出力を比較していき、サンプルデータSDSの方が大きければフリップフロップ52の蓄積値が更新されていくため、ピーク検出値PKは図4(e)のようになる。クリア信号CLRは磁気テープ90上の再生動作の1トラックに1回のタイミングで発生されることにより、1トラック単位でピーク検出値PKが得られる。

【0047】ピーク検出値PKは減算器34に供給され、目標値Mが減算される。そしてその減算により得られた誤差E、つまりピーク値と目標値Mの差がローパスフィルタ35に供給される。ローパスフィルタ35は、タイミング発生部33から図4(f)に示すようにクリア信号よりも所定期間遅延したタイミングでクロック(LPFクロック)CK_Lが供給されており、このLPFクロックCK_Lに基づいて平滑動作が行なわれる。つまり、フリップフロップ52のピーク検出値PKが正しく1トラック内のピーク値となったタイミングでの誤差Eが平滑処理対象となる。そしてローパスフィルタ35では、入力される誤差Eが近隣のトラック、つまり過去数トラック分についての誤差Eとの間で平滑化が行なわれ、その平滑化された信号EAVは乗算器36で係数αが乗算されてD/A変換器20に出力されることになる。

【0048】このような一連の動作の結果、ピーク検出値PKが目標値Mより小さい場合はD/A変換器20への出力値は小さくなり、これによりA/D変換器14のダイナミックレンジは小さくなる方向に修正される。逆にピーク検出値PKが目標値Mより大きければ、A/D変換器14のダイナミックレンジは大きくなる方向に修正される。

【0049】ここでサンプルデータSDが-128～+127の値をとるものとしたときに目標値Mを+110に設定したと考える。するとこの場合1トラック期間のサンプルデータSDのピーク値が平均して±110となるように制御されることになる。この場合、A/D変換器14での飽和に対する余裕率は、

$$\{(127-110)/110\} \times 100 = 15 (\%)$$

である。

【0050】一方、量子化誤差の増加を或る程度許容してでも飽和余裕率を増やしたいと考えるときは目標値Mを小さくすればよい。例えば目標値Mを+50に設定する。このときのA/D変換器14のダイナミックレンジは、A/D変換器14への入力信号振幅に対して大きくなる方向に変化されることになるため、飽和余裕率は増加する。即ち、

$$\{(127-50)/50\} \times 100 = 154 (\%)$$

となる。つまり、A/D変換器14への入力が突発的に2.54倍に大振幅化するまでは飽和しないことになる。

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【0051】以上のことから、A/D変換器14への入力として突発的な大振幅化が発生する恐れのある場合は、目標値Mの値を小さくして、飽和余裕を高くすれば良いことが理解される。そこで本例では制御信号発生部21は目標値Mとして使用できる値として、定常状態目標値M1と特殊状態目標値M2の2つの値を、それぞれスイッチ37のT1端子、T2端子に供給している。定常状態目標値M1は、比較的小さいダイナミックレンジを設定し、量子化誤差を少なくするための値とされ、例えばM1=「110」とされる。特殊状態目標値M2は、量子化誤差の増加を或る程度許容してでも飽和余裕を大きくするために比較的大きいダイナミックレンジを設定するための目標値であり、例えばM2=「50」とされる。

【0052】そして制御信号発生部21は上述したように、サーチ動作時、及び動作モード遷移時から所定期間において「H」となる特殊状態検出信号SSをスイッチ37の切換制御信号としてダイナミックレンジコントロール回路19に供給している。特殊状態検出信号SSが「H」となると、スイッチ37はT2端子が接続され、特殊状態検出信号SSが「L」となると、スイッチ37はT1端子が接続される。

【0053】特殊状態検出信号SSが「L」となっている期間とは、通常の再生動作時(定常状態)であり、このときは定常状態目標値M1が目標値Mとして減算器34に供給される。従って、M1=「110」とすると、上述のように飽和余裕率は15%であり、A/D変換器14のダイナミックレンジは入力信号に対して量子化誤差の少ない好適な状態に制御されることになる。一方、特殊状態検出信号SSが「H」となっている期間、即ちサーチ動作時、及び動作モード遷移時から所定期間では(特殊状態)、特殊状態目標値M2が目標値Mとして減算器34に供給される。従って、M1=「50」とすると、上述のように飽和余裕率は154%であり、A/D変換器14のダイナミックレンジは入力信号に対して量子化誤差は大きい十分な飽和余裕をもった状態に制御される。

【0054】図6にダイナミックレンジコントロールの様子を模式的に示す。時間軸方向(t1時点～t6時点)に動作モードが停止→再生→早送り(F F)→サーチ→巻戻(R E W)→サーチ→再生→停止と変化していったとする。図6(a)は目標値Mの変化、図6(b)は飽和余裕率の変化を示す。

【0055】最初に停止状態から再生が開始されてから一定期間(t0～t1)は特殊状態検出信号SSが「H」となるため、特殊状態目標値M2が目標値Mとして用いられ、ダイナミックレンジが大きく、つまり飽和余裕が大きくとられる。所定時間を経過し特殊状態検出信号SSが「L」となると(t1～t3)、定常状態目標値M1が目標値Mとして用いられ、ダイナミックレン

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シが小さく、飽和余裕は小さいが量子化誤差は小さい状態とされる。

【0056】さらに、12時点から早送りサーチに移行すると、特殊状態検出信号SSは「H」とされてダイナミックレンジが大きくされ、この状態は13～14時点の巻戻サーチも継続される。さらに14時点で再生動作に移行しても、モード変化から所定期間である15時点までは特殊状態検出信号SSは「H」のままであり、ダイナミックレンジが大きくされた状態は継続される。そして15時点以降16時点まではは定常状態として、ダイナミックレンジが小さく量子化誤差は小さい状態とされる。

【0057】即ち本例では、入力信号が或る程度安定している定常状態ではA/D変換器14のダイナミックレンジを小さくし、量子化誤差を少なくすることでエラーレートの向上をはかり、一方、サーチ時やモード変化時など、A/D変換器14への入力信号が突発的な変化を起こす恐れのあるときは、或る程度量子化誤差を許容しても、オーバーフローという最も避けなければならない事態が発生しないように、A/D変換器14のダイナミックレンジを大きくし、十分な飽和余裕をとるようすることでエラーが極度に増加することを防止するものである。

【0058】〔第2の実施の形態〕第2の実施の形態としての例を図7、図8で説明する。なお、記録再生装置としての全体の構成は図1と同様とし、図7には要部のみを示す。

【0059】この例におけるダイナミックレンジコントロール回路19で、上記第1の実施の形態でのダイナミックレンジコントロール回路19と異なる点は、スイッチ37がなく、制御信号発生部21から固定の目標値Mが減算器34に供給されていること、及び特殊状態検出信号SSはローパスフィルタ35に入力され、特殊状態検出信号SSがローパスフィルタ35の応答時定数を制御する動作を行なう点である。

【0060】ローパスフィルタ35は例えばIIRデジタルフィルタとして形成されるが、IIRデジタルフィルタの一般的なモデルを図8(a)に示す。即ち入力データは乗算器71で係数Kと乗算され、加算器72を介して遅延回路73で1サンプリング遅延されて出力される。遅延回路73の出力はまた乗算器74で係数(1-K)と乗算され、加算器72にフィードバックされる。このようなIIRデジタルフィルタでは、係数K(及び1-K)の値により応答時定数が変化することが知られている。

【0061】そこで本例では、特殊状態検出信号SSに基づいて係数K(及び1-K)の値を変化させるようにすることで、ダイナミックレンジ制御ループの応答速度を変換するようにしたものである。

【0062】特殊状態検出信号SSが「L」となってい

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る期間とは、上述したように通常の再生動作時(定常状態)であり、このときはA/D変換器14の入力としては急激な振幅変化はあらわれない。そしてダイナミックレンジ制御ループの安定性を向上させるためにはダイナミックレンジコントロール回路19としての応答性を或る程度遅くしたほうがよい。そこでローパスフィルタ35は、特殊状態検出信号SSが「L」となっている期間は、例えば係数 $K=0.1$ 、係数 $(1-K)=0.9$ と設定するようにする。するとローパスフィルタ35の応答時定数は図8(b)のように或る程度遅い状態とされる。

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【0063】一方、特殊状態検出信号SSが「H」となっている期間、即ちサーチ動作時、及び動作モード遷移時から所定期間では(特殊状態)、A/D変換器14の入力として急激な振幅変化が生ずる可能性がある。このような場合はダイナミックレンジコントロール動作としては即座に反応してオーバーフローや量子化誤差の増大を避ける必要がある。そこでローパスフィルタ35は、特殊状態検出信号SSが「H」となっている期間は、例えば係数 $K=0.3$ 、係数 $(1-K)=0.7$ と設定するようにし、応答時定数を図8(c)のように速い状態とする。

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【0064】このような本例では、サーチ時などでA/D変換器14の入力として急激な振幅変化が生じた場合には即座に反応してA/D変換器14のダイナミックレンジを適正に変化させ、オーバーフローや量子化誤差の増大を避けることができ、一方定常時には適度に遅い応答性によりダイナミックレンジ制御ループの安定性を実現することができる。

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【0065】〔第3の実施の形態〕第3の実施の形態としての例を図9で説明する。記録再生装置としての全体の構成は図1と同様とし、図9には要部のみを示す。この例が上述した第2の実施の形態としての例と異なる点は、正負評価部38を設けている点である。正負評価部38は減算器34の出力である誤差Eの値について、正値か負値かを判別し、その判別結果を時点数変更信号Jとしてローパスフィルタ35に供給する。

【0066】ダイナミックレンジコントロール19の動作としては、上述したように、ピーク検出値PKが目標値Mより小さい場合、即ち誤差Eが負の値であるときは、A/D変換器14のダイナミックレンジが小さくなるように制御を行ない、一方、ピーク検出値PKが目標値Mより大きい場合、即ち誤差Eが正の値であるときは、A/D変換器14のダイナミックレンジが大きくなるように制御を行なう。正負評価部38は、誤差Eの正負判断により、現在の処理はダイナミックレンジが大きくなるように制御を行なうのか、小さくなるように制御を行なうかを判別する。そして、その判別結果でローパスフィルタ35の時定数を制御することになる。

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【0067】誤差Eが負であると判別されたときは、ローパスフィルタ35は、例えば係数 $K=0.1$ 、係数 $(1-K)$

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$-K)=0.9$ と設定し、前述した図8(b)のようにローパスフィルタ35の応答時定数を或る程度遅い状態とする。一方、誤差Eが正であると判別されたときは、ローパスフィルタ35は例えば係数 $K=0.3$ 、係数 $(1-K)=0.7$ と設定するようにし、応答時定数を図8(c)のように遅い状態とする。

【0068】つまり本例のダイナミックレンジコントロール回路19では、A/D変換器14のダイナミックレンジを拡大するときには応答性を速くするものである。ダイナミックレンジを拡大するときとは、A/D変換器14への入力信号振幅が大きくなるときであり、つまりオーバーフローが生ずる可能性が発生する時である。従って、このようなときは迅速な応答性でダイナミックレンジの拡大制御を行なうことで、オーバーフロー発生を防止するものである。即ち、最も起こってはならないオーバーフローに対しての防止機能を強化するものであるといえる。

【0069】[第4の実施の形態] 第4の実施の形態の要部を図10に示す。この例におけるダイナミックレンジコントロール回路19の特徴としては、図1にも破線で示したようにデジタル等化回路15の出力についても監視するようにしている点である。この例では、A/D変換器14の出力であるサンプルデータSDは整流回路31Aに入力され、整流されたサンプルデータSDS1とされる。またデジタル等化回路15の出力は整流回路31Bに入力されて、同様に整流されたデータSDS2とされる。

【0070】整流回路31Aで整流されたサンプルデータSDS1はスイッチ40のTS1端子とコンパレータ39に供給される。また整流回路31Bで整流されたデータSDS2はスイッチ40のTS2端子とコンパレータ39に供給される。

【0071】コンパレータ39は入力されるデータSDS1、SDS2の値についての大小比較を行ない、その比較結果をスイッチ40に対する制御信号として出力する。即ちデータSDS1の方が大きければスイッチ40に端子TS1を接続させ、データSDS2の方が大きければスイッチ40に端子TS2を接続させる。

【0072】従って、A/D変換器14から出力されたサンプルデータSDとデジタル等化回路15の出力のうち、絶対値として大きいほうのデータがピーク検出回路32に供給され、ピーク検出動作の対象とされることになる。そして上述してきた各例と同様に、ピーク検出値PKと目標値Mが減算器34で減算され、得られた誤差Eに応じてダイナミックレンジの可変制御が行なわれる。

【0073】このような本例では、デジタル等化回路15もダイナミックレンジ制御ループに組み込まれることになる。仮にA/D変換器14においてオーバーフローが発生しなくても、デジタル等化回路15における演算

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でサンプルデータがオーバーフローする恐れもある。デジタル等化回路15におけるオーバーフローを防止するには、そのような恐れがあるときにA/D変換器14のダイナミックレンジを大きくすればよい。

【0074】そこで本例のようにデジタル等化回路15もダイナミックレンジ制御ループに組み込み、デジタル等化回路15の出力とA/D変換器14の出力の両方を監視して、ピーク検出を行なうことで、デジタル等化回路15でのオーバーフローも発生しないようにする。A/D変換器14のダイナミックレンジ制御が可能となる。

【0075】[第5の実施の形態] 第4の実施の形態の要部を図11に示す。この例は、ここまで説明してきた第1～第4の実施の形態としてのダイナミックレンジコントロール回路の特徴を全て備えるようにしたものである。

【0076】即ち第1の実施の形態と同様に、スイッチ37が特殊状態検出信号SSに応じて切り換わるようにし、つまり特殊状態検出信号SSにより目標値Mを定常状態目標値M1と特殊状態目標値M2に切り換えるようにする。これにより、定常再生状態では小さいダイナミックレンジで量子化誤差を少なく、またサーチ時、モード遷移時はダイナミックレンジを大きくして突発的な大幅入力に対しても飽和余裕が得られるようにする。

【0077】また第2の実施の形態と同様に、特殊状態検出信号SSによりローパスフィルタ35の応答時定数を変化させるとともに、第3の実施の形態と同様に誤差Eの正負評価に応じてローパスフィルタ35の応答時定数を変化させる。このため特殊状態検出信号SSはオアゲート41を介してローパスフィルタ35に供給され、また正負評価部38からの時定数変更信号Jもオアゲート41を介してローパスフィルタ35に供給される。

【0078】従って、サーチ時、モード遷移時にはローパスフィルタ35は高速応答状態とされ、さらにダイナミックレンジを拡大制御する際も高速応答状態とされる。これにより、A/D変換器14の入力として急激な振幅変化が生じても即座に定常してA/D変換器14のダイナミックレンジを適正に変化させ、オーバーフローや量子化誤差の増大を避けることができるように応答性を速くし、一方定常時には適度に遅い応答性としてダイナミックレンジ制御ループの安定性を得る。また、オーバーフローの恐れのあるダイナミックレンジ拡大時にも高速応答状態とされることで、オーバーフローを確実に回避できるようにしている。

【0079】さらに第4の実施の形態と同様にデジタル等化回路15の出力もダイナミックレンジ制御ループに取り込むようにしているため、A/D変換器14だけでなくデジタル等化回路15でのオーバーフロー防止という機能も発揮されることになる。

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【発明の効果】以上説明したように本発明のデータ再生装置では、A/D変換手段におけるダイナミックレンジを可変制御できるダイナミックレンジ制御手段として、当該データ再生装置の動作が定常状態であるときはダイナミックレンジを小さく、また当該データ再生装置の動作が特殊状態であるときはダイナミックレンジを大きくするように制御を行なうようにしている。このため、A/D変換手段のダイナミックレンジと入力信号レベルが常に適切な状態となるようにダイナミックレンジを可変制御されるとともに、突発的な振幅変化が殆ど発生しないと思われる定常状態では、A/D変換手段のダイナミックレンジを小さくして量子化誤差を小さくし、再生データとしてのエラーレートの向上を実現できる。また、突発的な振幅変化が発生する恐れのある特殊状態ではダイナミックレンジを大きくして飽和余裕を大きくし、少なくともオーバーフローを防止することが実現され、エラーが極度に増加することを防止できるという効果がある。特に特殊状態であるときは、当該データ再生装置がサーチ動作を行なっている期間や、動作モードが遷移したときの所定期間とすることが最もその効果が有効に発揮されることになる。

【0081】また、ダイナミックレンジ制御手段は、当該データ再生装置の動作が定常状態であるときはA/D変換手段の出力に応じたダイナミックレンジ可変制御動作の応答性が遅くなるように設定され、また当該データ再生装置の動作が特殊状態であるときはA/D変換手段の出力に応じたダイナミックレンジ可変制御動作の応答性が早くなるように設定することで、特殊状態において急激な振幅変化が生じた場合には即座に反応してダイナミックレンジを適正に変化させ、オーバーフローや量子化誤差の増大を避けることができる。また定常時には適度に遅い応答性によりダイナミックレンジ制御ループの安定性を実現することができるといふ効果がある。これについても特殊状態であるときは、当該データ再生装置がサーチ動作を行なっている期間や、動作モードが遷移したときの所定期間とすることで最もその効果が有効に発揮される。

【0082】さらに本発明では、ダイナミックレンジ制御手段は、A/D変換手段のダイナミックレンジを拡大する制御を行なう際には、A/D変換手段の出力に応じたダイナミックレンジ可変制御動作の応答性が早くなるように設定されるようにしている。つまりオーバーフローが生ずる可能性が発生するダイナミックレンジの拡大制御時に応答性を速くすることで、最も起こってはならないオーバーフローに対しての防止機能を強化することができるといふ効果がある。

【0083】さらに本発明では、A/D変換手段の出力と等化手段の出力の両方を監視して、A/D変換手段におけるダイナミックレンジを適応的に可変制御できるダイナミックレンジ制御手段を備えるようにしているた

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め、A/D変換手段と等化手段の両方について、オーバーフローが発生しないようにする制御が実現されるといふ効果がある。

【0084】そして以上のような効果から、本発明のデータ再生装置としては、定常動作時のエラーレートの向上、A/D変換手段と等化手段における飽和防止によるエラーレート悪化防止、制御ループ安定までの高速化により機器の再生性能、サーチ性能の向上、定常時の制御ループの安定性、等が実現される。また、このために付加する回路構成も簡易なもので実現できるという効果もある。

【図面の簡単な説明】

【図1】本発明の実施の形態の記録再生装置のブロック図である。

【図2】実施の形態の基本的なダイナミックレンジ制御動作の説明図である。

【図3】第1の実施の形態の要部のブロック図である。

【図4】実施の形態のダイナミックレンジコントロール回路の動作の説明図である。

【図5】実施の形態のピーク検出回路の回路図である。

【図6】実施の形態のダイナミックレンジコントロール動作の説明図である。

【図7】第2の実施の形態の要部のブロック図である。

【図8】実施の形態のローパスフィルタの応答性の説明図である。

【図9】第3の実施の形態の要部のブロック図である。

【図10】第4の実施の形態の要部のブロック図である。

【図11】第5の実施の形態の要部のブロック図である。

【図12】パーシャルレスポンス等化波形のアイパターンの説明図である。

【図13】サンプリングデータの分布状態の説明図である。

【図14】適正なダイナミックレンジ設定状態の説明図である。

【図15】ダイナミックレンジに比べて入力信号レベルが低い状態の説明図である。

【図16】ダイナミックレンジに比べて入力信号レベルが低い状態でのサンプリングデータの分布状態の説明図である。

【図17】ダイナミックレンジに比べて入力信号レベルが低い状態でのサンプリングデータの分布状態の説明図である。

【図18】ダイナミックレンジに比べて入力信号レベルがより低い状態でのサンプリングデータの分布状態の説明図である。

【図19】ダイナミックレンジに比べて入力信号レベルがより低い状態でのサンプリングデータの分布状態の説明図である。

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【図20】ダイナミックレンジに比べて入力信号レベルが極度に低い状態でのサンプリングデータの分布状態の説明図である。

【図21】ダイナミックレンジに比べて入力信号レベルが極度に低い状態でのサンプリングデータの分布状態の説明図である。

【図22】ダイナミックレンジに比べて入力信号レベルが大きい状態でのサンプリングデータの分布状態の説明図である。

【図23】ダイナミックレンジに比べて入力信号レベルが大きい状態の説明図である。

【図24】ダイナミックレンジに比べて入力信号レベルがさらに大きい状態でのサンプリングデータの分布状態の説明図である。

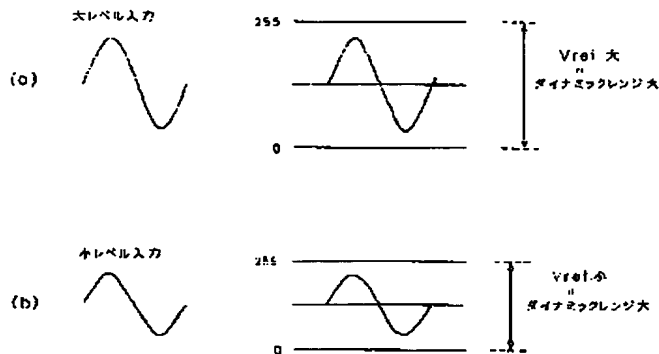
【図25】ダイナミックレンジに比べて入力信号レベル*

*がさらに大きい状態の説明図である。

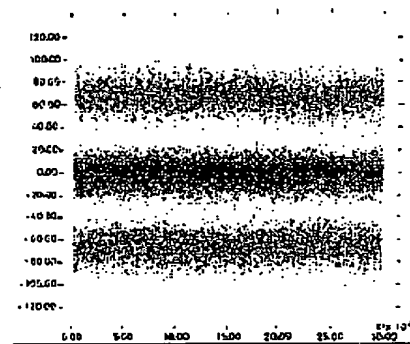
【符号の説明】

4 8-10変調部、5 プリコーダ、6 記録アンプ、7、10 ロータリーエンコーダ、8 記録ヘッド、9 再生ヘッド、11 再生アンプ、12 アナログ等化回路、13 PLL回路、14 A/D変換器、15 デジタル等化回路、16 2値化回路、17 10-8変換部、18 エラー訂正部、19ダイナミックレンジコントロール回路、20 D/A変換器、21 制御信号発生部、31、31A、31B 整流回路、32 ピーク検出回路、33 タイミング発生部、34 減算器、35 ローパスフィルタ、36 乗算器、37、40 スイッチ、38 正負評価部、39 コンパレータ、41 オアゲート

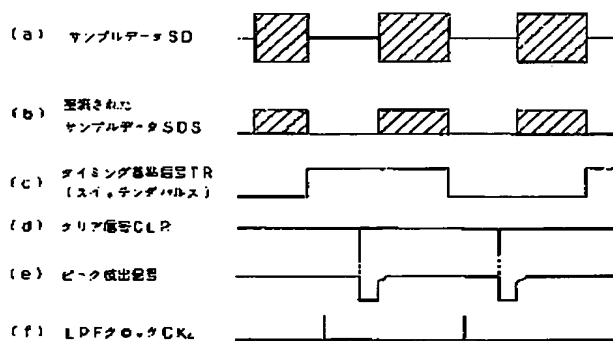
【図2】



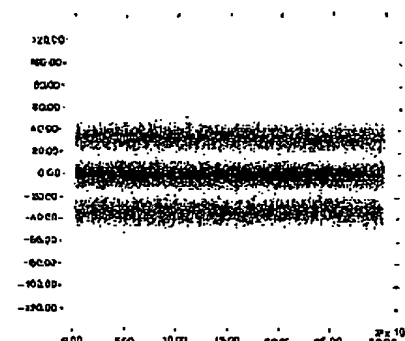
【図13】



【図4】



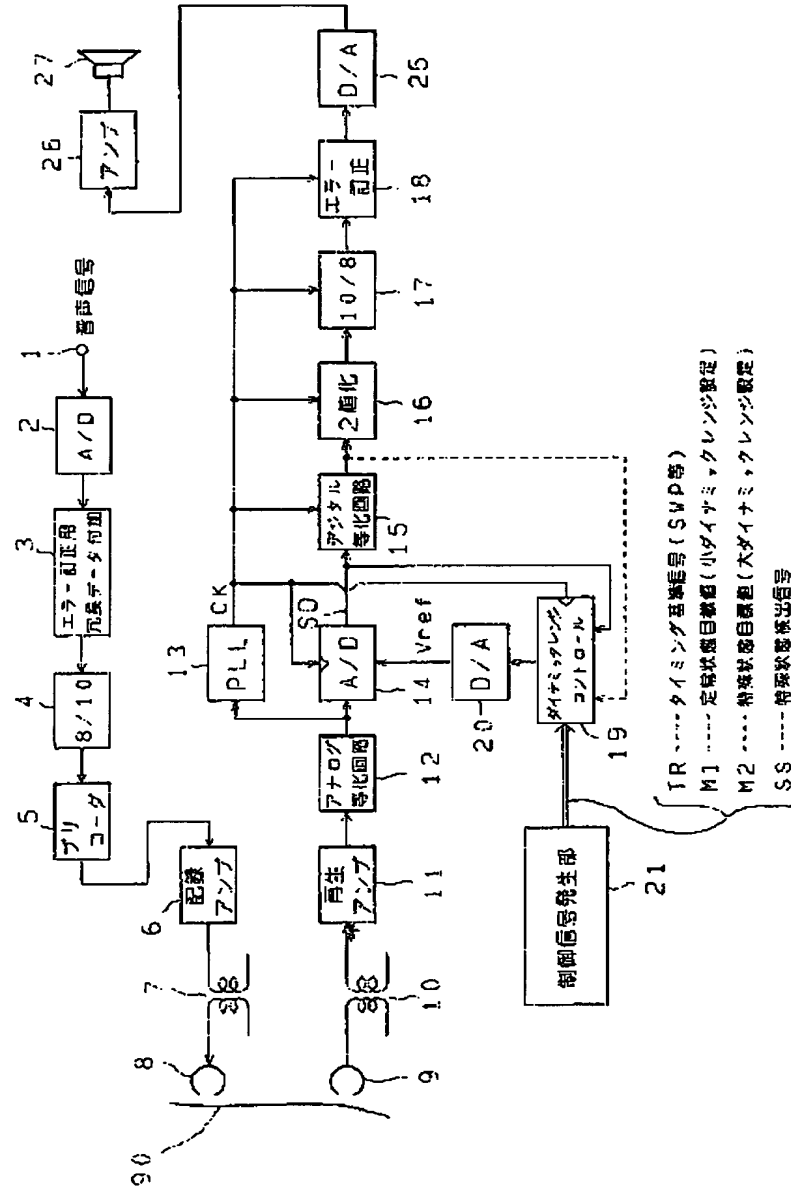
【図16】



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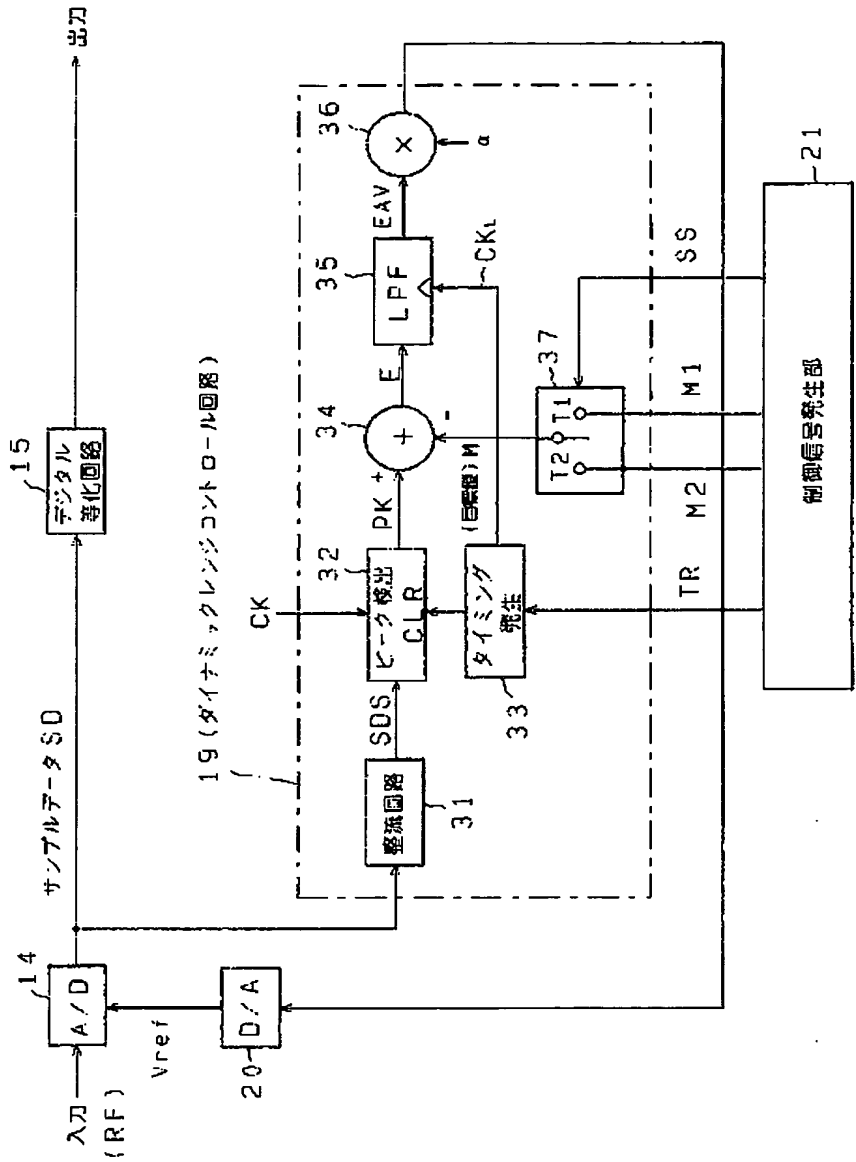
【図1】



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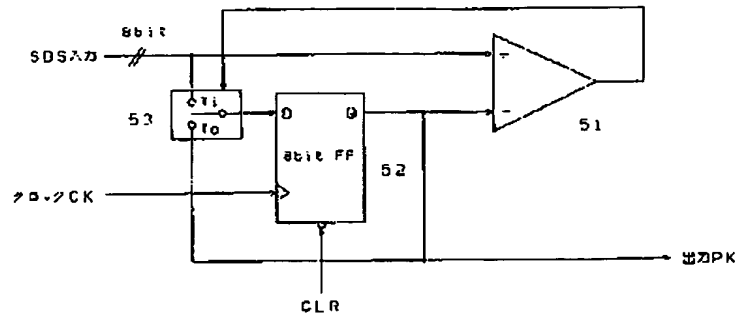
【図3】



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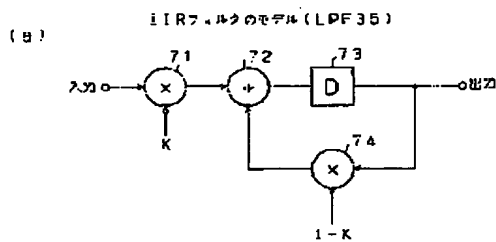
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【図5】

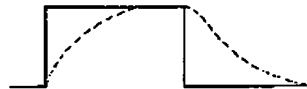


ピーク検出回路32

【図8】

(b) $K=0.1$, $1-K=0.9$

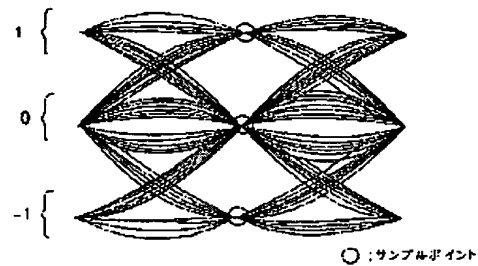
安定数: 遅

(c) $K=0.3$, $1-K=0.7$

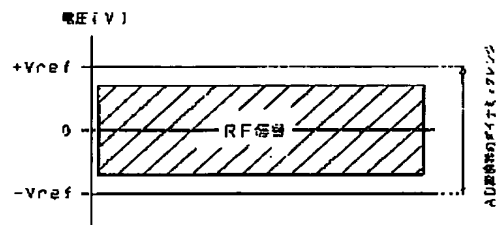
安定数: 速



【図12】



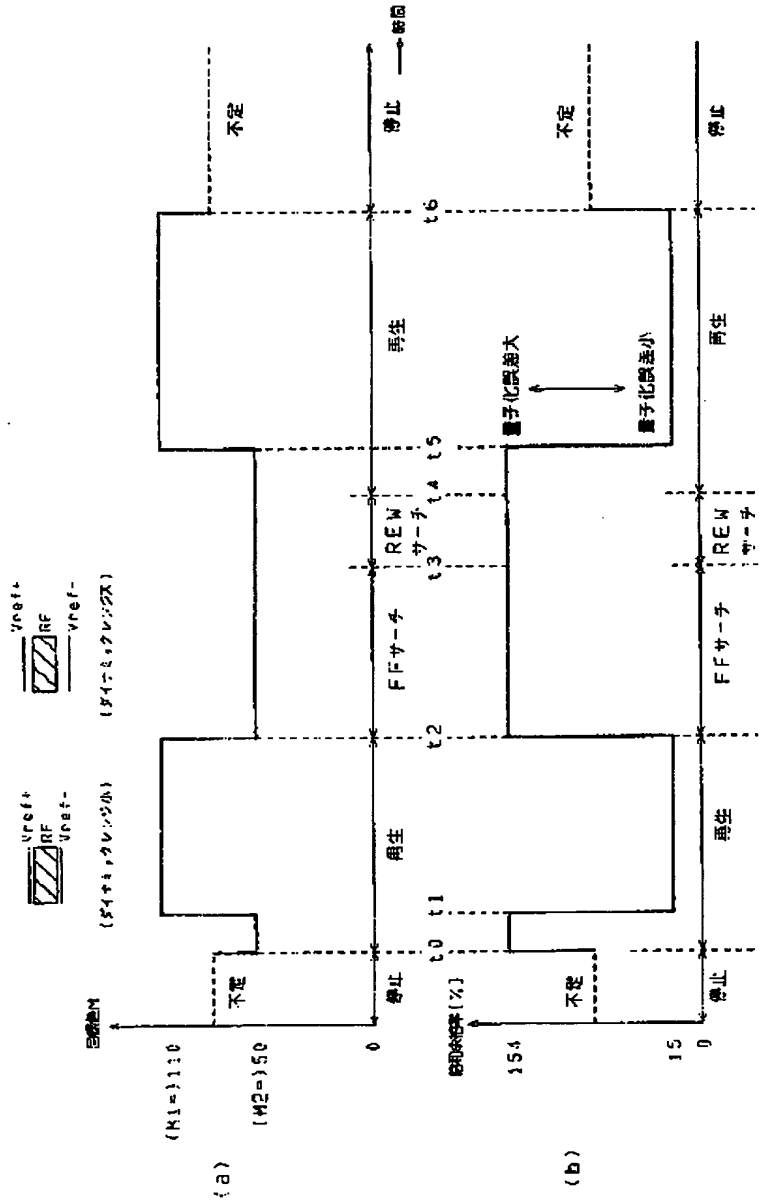
【図14】



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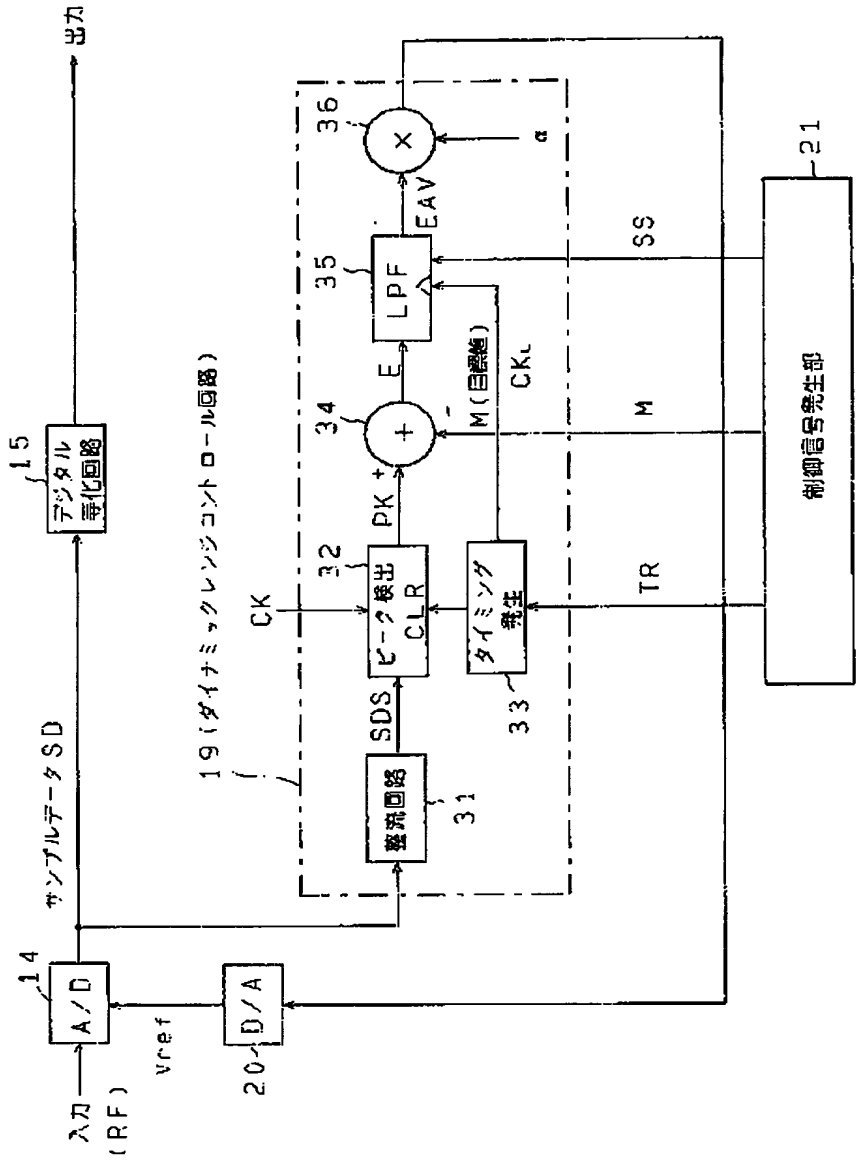
【図6】



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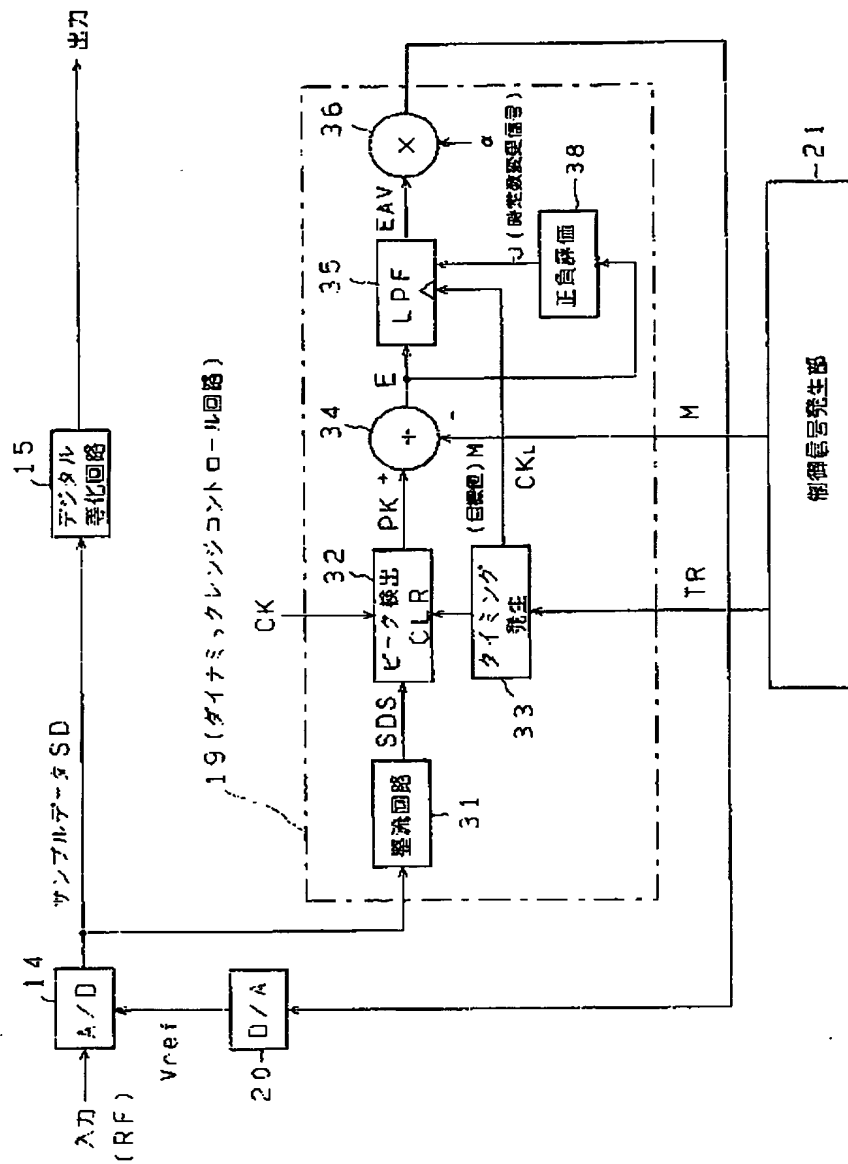
【図7】



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(17)

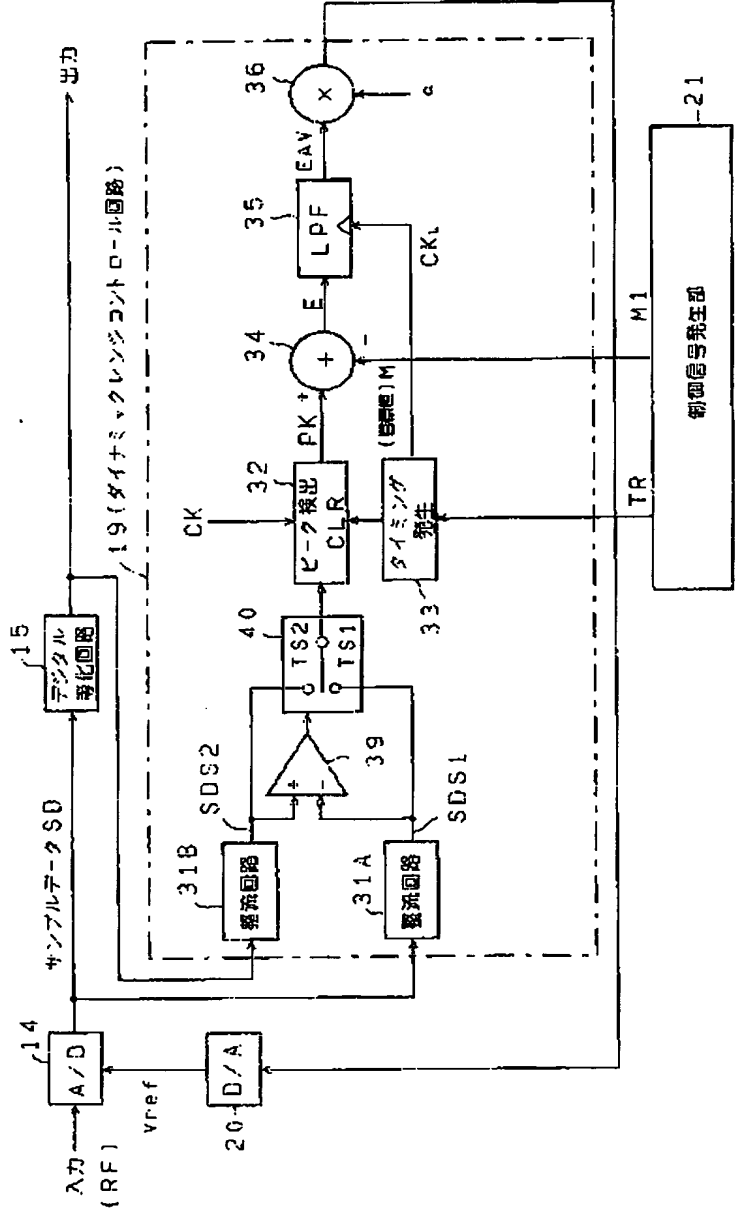
【図9】



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(18)

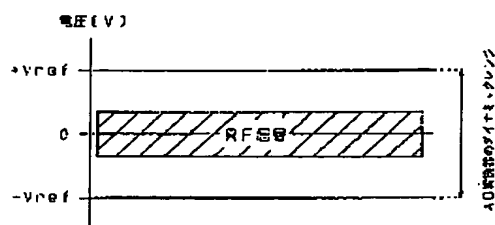
【図10】



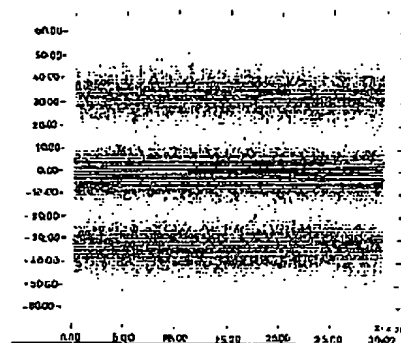
(20)

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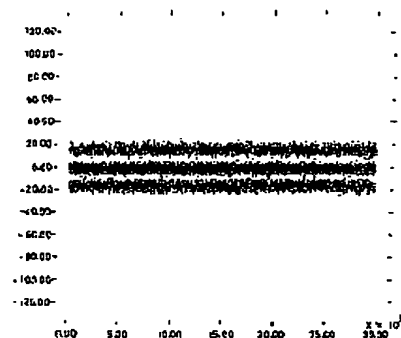
【図15】



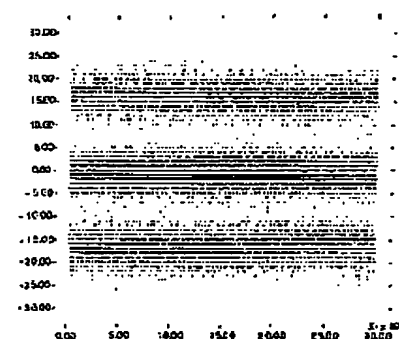
【図17】



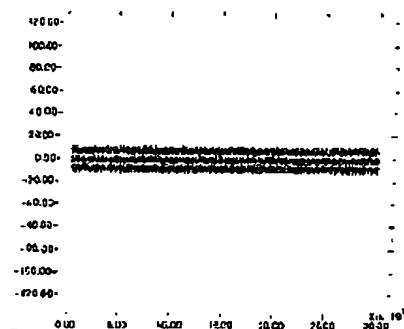
【図18】



【図19】



【図20】



【図21】

